Sardar Patel Institute of Technology

Bhavan's Campus, Munshi Nagar, Andheri (West), Mumbai-400058-India
(Autonomous Institute Affiliated to University of Mumbai)

Course Code	Course Name	Teaching Scheme (Hrs/week)			Credits Assigned			
		L	T	P	L	T	P	Total
EXL7053	ASIC Verification Lab	--	--	2	--	--	1	1
		Examination Scheme						
		ISE			ESE			Total
					Practical		Oral	
		40			--		20	60

Pre-requisite Course Codes		EXC7053 (ASIC Verification)
After successful completion of the course, student will be able to		
Course Outcomes	CO1	Install and use modern tools available for verification
	CO2	Compose the SystemVerilog code for verification
	CO3	Construct testbench for verification
	CO4	Investigate the given verification code
	CO5	Validate the code under constrained environments
	CO6	Debate the results of verification tool

Exp. No.	Experiment Details	Ref.	Marks
1	1. Simulate verilog code for a. D Flip-Flop (Using EDA Playground) b. 2:1 Mux : Using case Statement c. 4-bit Ripple Carry Full Adder by instantiating one bit full adder d. D Flip Flop using gates e. Example for blocking and non-blocking statements f. 8-Bit Up Counter With Load Do simulation, synthesis, implementation and physical verification of any one of above Verilog design of your choice on given CPLD/FPGA platform.	1,2	5
2	Complete the given task on literals and data types in SystemVerilog Also write the simulation output for the given Procedural Statements	3,4	5
3	Write the simulation output for the given Interprocess Communication	3,4	5
4	Write the simulation output for the given randomization code	3,4	5
5	Write the simulation output for the given Interfaces, Program and Clocking Blocks	3,4	5
6	Write the simulation output for the given Processes	3,4	5
7	Write the simulation output for the given Functional Coverage	3,4	5
8	Write the simulation output for the given Assertions	3,4	5
	Total Marks		**40**

References:

[1] Spartan and Virtex family user manuals from Xilinx

[2]Verilog Language Reference manual

[3]System Verilog Language Reference manual

[4] Chris Spear, "System Verilog for Verification: A guide to learning the testbench language features", Springer, 2nd Edition