Sardar Patel Institute of Technology

Bhavan's Campus, Munshi Nagar, Andheri (West), Mumbai-400058-India
(Autonomous Institute Affiliated to University of Mumbai)

Course Code	Course Name	Teaching Scheme (Hrs/week)			Credits Assigned			
		L	T	P	L	T	P	Total
EXC7053	ASIC Verification	4	--	--	4	--	--	4
		Examination Scheme						
		ISE		MSE		ESE		
		10		30		100 (60% Weightage)		

Pre-requisite Course Codes		EXL304: Object Oriented Programming Methodology Laboratory EXC303: Digital Circuits and Design
After successful completion of the course, student will be able to		
Course Outcomes	CO1	Recognise trends in ASIC verification
	CO2	Apply SystemVerilog constructs for verification
	CO3	Create testbenches, threads and show interprocess communication
	CO4	Create test cases under constrained environment
	CO5	Validate design with SystemVerilog assertions and functional coverage
	CO6	Interface SystemVerilog with other languages

Module No.	Unit No.	Topics	Ref.	Hrs.
1		**Programmable Devices and Verilog**		08
	1.1	**Programmable Devices:** Architecture of FPGA, CPLD with an example of Virtex-7 and Spartan -6 family devices	6	
	1.2	**Verilog HDL:** Data types, expressions, assignments, behavioral, gate and switch level modeling, tasks and functions	7	
	1.3	**Verification Basics:** Technology challenges, Verification methodology options, Verification methodology, Testbench creation, testbench migration, Verification languages, Verification IP reuse, Verification approaches, Verification and device test, Verification plans, reference design of Bluetooth SoC, Verification Guidelines	1,5	
2		**Data types, procedural statements and testbench**		08
	2.1	**Data Types:** Built in, Fixed size array, dynamic array, queues, associative array, linked list, array methods, choosing a storage type, creating new types with typedef, creating user-defined structures, type conversion, enumerated types, constants, strings, expression width	1,2,4	
	2.2	**Procedural Statements and Routines:** Procedural statements, tasks, functions and void functions, task and function overview, routine arguments, returning from a routine, local data storage, time values	1,2,4	
	2.3	**Connecting the Testbench and Design:** Separating the testbench and design, the interface construct, stimulus timing, interface driving and sampling, connecting it all together, top-level scope, program-module interactions, system verilog assertions, the four port ATM router, the ref port direction, the end of simulation, directed test for the LC3 fetch	1,2,4	

		block		
3		**OOP and Randomization**		**10**
	3.1	**Basic OOP:** Class, Creating new objects, Object deallocation, using objects, variables, class methods, defining methods outside class, scoping rules, using one class inside another, understanding dynamic objects, copying objects, public vs. local, building a testbench	1,2,4	
	3.2	**Randomization:** Randomization in system Verilog, constraint details, solution probabilities, controlling multiple constraint blocks, valid constraints, In-line constraints, The pre-randomize and post-randomize functions, Random number functions, Constraints tips and techniques, common randomization problems, Iterative and array constraints, Atomic stimulus generation vs. scenario generation, random control, random number generators, random device configuration	1,2,4	
4		**IPC and advanced OOP**		**08**
	4.1	**Threads and Interprocess Communication:** working with threads, disabling threads, interprocess communication, events, semaphores, mailboxes, building a testbench with threads and IPC	1,2,4	
	4.2	**Advanced OOP and Testbench Guidelines:** Inheritance, Blueprint pattern, downcasting and virtual methods, composition, inheritance and alternatives, copying an object, abstract classes and pure virtual methods, callbacks, parameterized classes	1,2,4	
5		**Assertions and Functional Coverage**		**12**
	5.1	**System Verilog Assertions:** Assertions in verification methodology, Understanding sequences and properties, SystemVerilog Assertions in the Design Process, Formal Verification Using Assertions and SystemVerilog Assertions Guidelines	3	
	5.2	**Functional Coverage:** Coverage types, strategies, examples, anatomy of a cover group, triggering a cover group, data sampling, cross coverage, generic cover groups, coverage options, analyzing coverage data, measuring coverage statistics during simulation	1,2,4	
6		**Advanced interfaces and interfacing with C**		**06**
	6.1	**Advanced Interfaces:** Virtual interfaces with the ATM router, Connecting to multiple design configurations, procedural code in an interface	1,2,4	
	6.2	**A complete System Verilog Testbench:** Design blocks, testbench blocks, alternate tests	1,2,4	
	6.3	**Interfacing with C:** Passing simple values, connecting to a simple C routine, connecting to C++, simple array sharing, open arrays, sharing composite types, pure and context imported methods, communicating from C to system verilog, connecting other languages	1,2,4	
			Total	**52**

References:

[1] Chris Spear, "System Verilog for Verification: A guide to learning the testbench language features", Springer, Second Edition

[2] Stuart Sutherland, Simon Davidmann, and Peter Flake, "System Verilog for Design: A guide to using system verilog for hardware design and modeling", Springer, Second Edition.

[3] Ben Cohen, Srinivasan Venkataramanan, Ajeetha Kumari and Lisa Piper, "SystemVerilog Assertions Handbook", VhdlCohen Publishing, Third edition

[4] System Verilog Language Reference manual

[5] S Prakash Rashinkar, Peter Paterson and Leena Singh, "System on Chip Verification Methodologies and Techniques", Kluwer Academic, First Edition.

[6] Spartan and Virtex family user manuals from Xilinx

[7] Verilog Language Reference manual