Sardar Patel Institute of Technology

Bhavan's Campus, Munshi Nagar, Andheri (West), Mumbai-400058-India
(Autonomous Institute Affiliated to University of Mumbai)

Course Code	Course Name	Teaching Scheme (Hrs/week)			Credits Assigned			
		L	T	P	L	T	P	Total
EXL702	IC Technology Laboratory	--	--	2	--	--	1	1
		Examination Scheme						
		ISE			ESE			Total
					Practical		Oral	
		40			--		20	60

Pre-requisite Course Codes		EXC702 (IC Technology)
After successful completion of the course, student will be able to		
Course Outcomes	CO1	Make use of modern tools available for process and layout simulation
	CO2	Compose simulation program for a fabrication process to arrive at valid conclusion
	CO3	Draw layout and sketch characteristics of MOS circuit to arrive at valid conclusion
	CO4	Validate device characteristics via simulations to arrive at valid conclusion
	CO5	Build layout as per the design rules

Exp. No.	Experiment Details	Ref.	Marks
1	Draw and simulate layout for the CMOS inverter. Carry out static as well as transient simulation. Analyze CMOS inverter for i) (W/L)pmos>(W/L)nmos ii) (W/L)pmos=(W/L)nmos iii) (W/L)pmos<(W/L)nmos. Do parasitic extraction. Feed these parasitic in circuit simulator and do layout versus schematic verification.	3,5	5
2	Draw and simulate layout for the following circuits. Size them with respect to reference inverter. a. CMOS NAND b. CMOS NOR Also observe the effect of different types of design rules on above circuits and tabulate the comparative results	3,5	5
3	Draw and simulate layout for the given equation (each student will get different equation [y= $\overline{A.B + C.D}$]) with the following design style a. Static CMOS b. Transmission gate c. Dynamic Logic	3,5	5
4	Simulate n type and p type MOSFETs (bulk, SOI and Double Gate) to obtain family of ID-VG and ID-VD characteristics. Compare the results obtained. (Tool: a TCAD lab on nanohub.org)	1,4	5
5	Simulate Carbon Nanotube MOSFET for different conditions (e.g. gate/drain voltage sweep, threshold voltage etc.) and comment on the	1,3	5

	1,3results obtained. (Tool: FETToy on nanohub.org)		
6	Simulate Silicon Nanowire MOSFET for different conditions (e.g. gate/drain voltage sweep, threshold voltage etc.) and comment on the results obtained. (Tool: FETToy on nanohub.org)	1,3	**5**
7	Simulate FinFET to plot energy band diagram and IV characteristics for different values of gate and drain bias. Comment on the results obtained. (Tool: MuGFET on nanohub.org)	4	**5**
8	Simulate SOI MOSFET and plot its characteristics. (Tool: Visual TCAD/Mentor)	2, 4	**5**
		Total Marks	**40**

References:

[1] *www.nanohub.org*

[2] Visual TCAD lab manual

[3] James D. Plummer, Michael D. Deal and Peter B. Griffin, "*Silicon VLSI Technology*", Pearson, Indian Edition

[4] Jean-Pierre Colinge, "*FinFETs and Other Multigate Transistors",* Springer, 1st edition

[5] Microwind User Manual