Sardar Patel Institute of Technology

Bhavan's Campus, Munshi Nagar, Andheri (West), Mumbai-400058-India
(Autonomous Institute Affiliated to University of Mumbai)

Course Code	Course Name	Teaching Scheme (Hrs/week)			Credits Assigned			
		L	T	P	L	T	P	Total
EXC702	IC Technology	4	--	--	4	--	--	4
		Examination Scheme						
		ISE		MSE		ESE		
		10		30		100 (60% Weightage)		

Pre-requisite Course Codes		EXC302: Electronic Devices EXC303: Digital Circuits and Design EXC402: Discrete Electronic Circuits EXC502: Design With Linear Integrated Circuits EXC601: VLSI Design
At the end of successful completion of the course, student will be able to		
Course Outcomes	CO1	Discuss integrated circuit fabrication processes
	CO2	Illustrate the sequence of process of semiconductor device fabrication
	CO3	Discuss the semiconductor parameter measurement techniques
	CO4	Interpret the physical mechanism of novel semiconductor devices
	CO5	Summarize features of novel semiconductor devices and justify use of these devices in an application

Module No.	Unit No.	Topics	Ref.	Hrs.
1		**Environment and Crystal Growth for VLSI Technology**		08
	1.1	**Environment:** Semiconductor technology trend, Clean rooms, Wafer cleaning	1,2,3,4	
	1.2	**Semiconductor Substrate:** Phase diagram and solid solubility, Crystal structure, Crystal defects, Czochralski growth, Bridgman growth of GaAs, Float Zone growth, Wafer Preparation and specifications	1,2,3,4	
2		**Fabrication Processes Part 1**		10
	2.1	**Deposition:** Evaporation, Sputtering and Chemical Vapor Deposition	1,2,3,4	
	2.2	**Epitaxy:** Molecular Beam Epitaxy, Vapor Phase Epitaxy, Liquid Phase Epitaxy, Evaluation of epitaxial layers	1,2,3,4	
	2.3	**Silicon Oxidation:** Thermal oxidation process, Kinetics of growth, Properties of Silicon Dioxide, Oxide Quality, high κ and low κ dielectrics	1,2,3,4	
	2.4	**Diffusion:** Nature of diffusion, Diffusion in a concentration gradient, diffusion equation, impurity behavior, diffusion systems, problems in diffusion, evaluation of diffused layers	1,2,3,4	
	2.5	**Ion Implantation:** Penetration range, ion implantation systems, process considerations, implantation damage and annealing	1,2,3,4	
3		**Fabrication Processess Part 2**		10
	3.1	**Etching:** Wet chemical etching, dry physical etching, dry chemical	1,2,3,4	

		etching, reactive ion etching, ion beam techniques		
	3.2	**Lithography:** Photoreactive materials, Pattern generation and mask making, pattern transfer, Electron beam, Ion beam and X-ray lithography	1,2,3,4	
	3.3	**Device Isolation, Contacts and Metallization:** Junction and oxide isolation, LOCOS, trench isolation, Schottky contacts, Ohmic contacts, Metallization and Packaging	1,2,3,4	
	3.4	**CMOS Process Flow:** N well, P-well and Twin tub	1,2,3,4	
	3.5	Design rules, Layout of MOS based circuits (gates and combinational logic), Buried and Butting Contact	1,2,3,4	
4		**Measurements, Packaging and Testing**		**10**
	4.1	**Semiconductor Measurements:** Conductivity type, Resistivity, Hall Effect Measurements, Drift Mobility, Minority Carrier Lifetime and diffusion length	7	
	4.2	**Packaging:** Integrated circuit packages, Electronics package reliability	9	
	4.3	**Testing:** Technology trends affecting testing, VLSI testing process and test equipment, test economics and product quality	10	
5		**SOI, GaAs and Bipolar Technologies**		**8**
	5.1	**SOI Technology:** SOI fabrication using SIMOX, Bonded SOI and Smart Cut, PD SOI and FD SOI Device structure and their features	5	
	5.2	**GaAs Technologies:** MESFET Technology, Digital Technologies, MMIC technologies, MODFET and Optoelectronic Devices	8	
	5.3	**Silicon Bipolar Technologies:** Second order effects in bipolar transistor, Performance of BJT, Bipolar processes and BiCMOS	8	
6		**Novel Devices**		**6**
	6.1	**Multigate Device:** Various multigate device configurations (device structure and important features)	6	
	6.2	**Nanowire:** Fabrication and applications	8	
	6.3	**Graphene Device:** Carbon nanotube transistor fabrication, CNT applications	8	
			Total	**52**

References:

[1] James D. Plummer, Michael D. Deal and Peter B. Griffin, "Silicon VLSI Technology", Pearson, Indian Edition.

[2] Stephen A. Campbell, "The Science and Engineering of Microelectronic Fabrication", Oxford University Press, Second Edition.

[3] Sorab K. Gandhi, "VLSI Fabrication Principles", Wiley, Student Edition.

[4] G. S. May and S. M. Sze, "Fundamentals of Semiconductor Fabrication", Wiley, First Edition.

[5] Kerry Bernstein and N. J. Rohrer, "SOI Circuit Design Concepts", Kluwer Academic Publishers, First edition.

[6] Jean-Pierre Colinge, "FinFETs and Other Multigate Transistors", Springer, First edition

[7] M. S. Tyagi, "Introduction to Semiconductor Materials and Devices", John Wiley and Sons, First Edition.

[8] James E. Morris and Krzysztol Iniewski, "Nanoelectronic Device Applications Handbook", CRC Press

[9] Glenn R. Blackwell, "The electronic packaging", CRC Press

[10] Michael L. Bushnell and Vishwani D. Agrawal, "Essentials of Electronic Testing for digital, memory and mixed-signal VLSI circuits", Springer