Sardar Patel Institute of Technology

Bhavan's Campus, Munshi Nagar, Andheri (West), Mumbai-400058-India
(Autonomous Institute Affiliated to University of Mumbai)

Course Code	Course Name	Teaching Scheme (Hrs/week)			Credits Assigned			
		L	T	P	L	T	P	Total
EXC801	CMOS VLSI Design	4	--	--	4	--	--	4
		Examination Scheme						
		ISE		MSE		ESE		
		10		30		100 (60% Weightage)		

Pre-requisite Course Codes		EXC302: Electronic Devices EXC303: Digital Circuits and Design EXC402: Discrete Electronic Circuits EXC502: Design With Linear Integrated Circuits EXC601: VLSI Design EXC702: IC Technology
After successful completion of the course, student will be able to		
Course Outcomes	CO1	Recognize tradeoffs involved in analog VLSI Circuits
	CO2	Analyze basic building blocks of CMOS analog VLSI circuits
	CO3	Evaluate MOSFET based single stage and differential amplifiers
	CO4	Design MOSFET based operational amplifier
	CO5	Analyze mixed signal circuits
	CO6	Describe layout techniques for analog circuits

Module No.	Unit No.	Topics	Ref.	Hrs.
1		**CMOS analog building blocks**		08
	1.1	**MOS Models:** Necessity of CMOS analog design, Review of characteristics of MOS device, MOS small signal model, MOS spice models	1	
	1.2	**Passive and Active Current Mirrors:** Basic current mirrors, Cascode current mirrors and Active current mirrors	1	
	1.3	**Band Gap References:** General Considerations, Supply-independent biasing, Temperature independent references, PTAT current generation and Constant Gm biasing	1	
2		**Single Stage Amplifiers**		10
	2.1	**Configurations:** Basic concepts, Common source stage, Source follower, Common gate stage, Cascode stage	1	
	2.2	**Frequency Response and Noise:** General considerations, Common-source stage, Source followers, Common-gate stage, Cascode stage and Noise in single stage amplifiers	1	
3		**Differential Amplifiers**		10
	3.1	**Configurations:** Single ended and differential operation, Basic differential pair, Common-mode response, Differential pair with MOS loads, Gilbert cell	1	
	3.2	Frequency response and noise in differential pair	1	

4		**MOS Operational Amplifiers**		**10**
	4.1	**Op-amp Design:** General Considerations, performance parameters, One-stage op-amps, Two-stage op-amps, Gain Boosting, Common-mode feedback, Input range limitations, Slew Rate, Power supply rejection, Noise in op-amps	1,3,5	
	4.2	**Stability and Frequency Compensation:** General Considerations, Multipole systems, Phase margin, Frequency compensation, compensation of two stage op-amps	1	
5		**Mixed Signal Circuits**		**10**
	5.1	**Switch Capacitor Circuits:** MOSFETs as switches, Speed considerations, Precision Considerations, Charge injection cancellation, Unity gain buffer, Non-inverting amplifier and integrator	1	
	5.2	**Oscillators:** General considerations, Ring oscillators, LC oscillators, VCO	1	
	5.3	**Phase-Locked Loop:** Simple PLL, Charge pump PLL, Nonideal effects in PLL, Delay locked loops and applications of PLL in integrated circuits	1	
6		**Analog Layout and other concepts**		**04**
	6.1	**Analog Layout Techniques:** Antenna effect, Resistor matching, capacitor matching, current mirror matching, floorplanning, shielding and guard rings	1,2	
	6.2	AMS design flow, ASIC, Full custom design, Semi custom design, System on Chip, System in package, Hardware software co-design	1	
			Total	**52**

References:

[1] B Razavi, "Design of Analog CMOS Integrated Circuits", Tata McGraw Hill, First Edition.

[2] R. Jacaob Baker, Harry W. Li, David E. Boyce, "CMOS Circuit Design, Layout,and Stimulation", Wiley, Student Edition

[3] P. E. Allen and D. R. Holberg, "CMOS Analog Circuit Design", Oxford University Press, Third Edition.

[4] Gray, Meyer, Lewis, Hurst, "Analysis and design of Analog Integrated Circuits", Willey, Fifth Edition