Sardar Patel Institute of Technology

Bhavan's Campus, Munshi Nagar, Andheri (West), Mumbai-400058-India
(Autonomous Institute Affiliated to University of Mumbai)

Course Code	Course Name	Teaching Scheme (Hrs/week)			Credits Assigned			
		L	T	P	L	T	P	Total
ETE704	Analog and Mixed Signal VLSI	4	--	--	4	--	--	4
		Examination Scheme						
		ISE		MSE		ESE		
		10		30		100 (60% Weightage)		

Pre-requisite Course Codes		ETC302: Analog Electronics I ETC303. Digital Electronics ETC402: Analog Electronics II ETC 505: Integrated Circuits ETC 606 :VLSI Design
After successful completion of the course, student will be able to		
Course Outcomes	CO1	Differentiate between Analog, Digital and Mixed Signal CMOS Integrated Circuits.
	CO2	Analyze and design current sources and voltage references for given specifications
	CO3	Analyze and design single stage MOS Amplifiers
	CO4	Analyze and design Operational Amplifiers.
	CO5	Analyze and design data converter circuits.

Module No.	Unit No.	Topics	Ref.	Hrs.
1	**Fundamental Analog Building Blocks**			08
	1.1	MOS Transistor as sampling switch, active resistances, current source and sinks, current mirror and current amplifiers		
	1.2	Voltage and current references, band gap voltage reference, Beta-Multipler referenced self-biasing		
2	**Single Stage MOS Amplifiers**			14
	2.1	Common-source stage (with resistive load, diode connected load, current-source load, triode load, source degeneration), source follower, common-gate stage, cascode stage, folded cascade stage, simulation of CMOS amplifiers using SPICE		
	2.2	Single-ended operation, differential operation, basic differential pair, large-signal and small-signal behavior, common-mode response, differential pair with MOS loads, simulation of differential amplifiers using SPICE		
	2.3	Noise characteristics in the frequency and time domains, thermal noise, shot noise, flicker noise, popcorn noise, noise models of IC components, representation of noise in circuits, noise in single-stage amplifiers (CS, CD and CG stages), noise in differential pairs, noise		

		bandwidth, noise figure, noise temperature.		
3	**MOS Operational Amplifiers Desing**			08
	3.1	Trans-conductance operational amplifier (OTA), two stage CMOS operational amplifier		
	3.2	CMOS operational amplifiers compensation, cascade operational amplifier and folded cascade		
4	**Non-Linear & Dynamic Analog Circuits**			08
	4.1	Switched capacitor amplifiers (SC), switched capacitor integrators, first and second order switched capacitor circuits.		
	4.2	Basic CMOS comparator design, adaptive biasing, analog multipliers		
5	**Data Converter Fundamentals**			06
	5.1	Analog versus digital discrete time signals, converting analog signals to data signals, sample and hold characteristics		
	5.2	DAC specifications, ADC specifications, mixed-signal layout issues		
6	**Data Converter Architectures**			08
	6.1	DAC architectures, digital input code, resistors string, R-2R ladder networks, current steering, charge scaling DACs, Cyclic DAC, pipeline DAC.		
	6.2	ADC architectures, flash, 2-step flash ADC, pipeline ADC, integrating ADC, and successive approximation ADC		
			Total	**52**

References:

1. B. Razavi, **"***Design of Analog CMOS Integrated Circuits***"**, first edition, McGraw Hill,2001.
2. Harry W. Li and David E Boyce, **"***CMOS Circuit Design, Layout, Stimulation***",** PHI Edn, 2005
3. P.E.Allen and D R Holberg, **"***CMOS Analog Circuit Design***"**, second edition, Oxford University Press, 2002.
4. Gray, Meyer, Lewis and Hurst **"***Analysis and design of Analog Integrated Circuits***"**, 4th Edition Willey International, 2002