



Sardar Patel Institute of Technology

Bhavan's Campus, Munshi Nagar, Andheri (West), Mumbai-400058-India
(Autonomous Institute Affiliated to University of Mumbai)

Course Code	Course Name	Teaching Scheme (Hrs/week)			Credits Assigned				
		L	T	P	L	T	P	Total	
CEL32	Digital Logic Design & Analysis Lab	-	-	2	-	-	1	1	
		Examination Scheme							Total
		ISE		ESE		Total			
		40		Practical	Oral		10	10	60

Pre-requisite Course Codes	ES11 (Basic Electrical and Electronics Engineering) CE32 (Digital Logic Design and Analysis)
After successful completion of the course, student will be able to:	
Course Outcomes	CO1 Construct and test logic circuits using logic gates to realize given function.
	CO2 Construct and Test logic circuits using MSI ICs to realize given function.
	CO3 Validate and test the design of combinational and sequential logic circuits by hardware implementation.
	CO4 Develop an application using concepts of digital circuits.

Exp. No.	Experiment Details	Ref.	Marks
1	To implement the combinational logic for given function using basic gates/MSI ICs.	1,2	5
2	To interface TTL and CMOS logic families with each other.	1,2	5
3	To implement 4-bit, 5-bit and 8 bit comparator using MSI ICs	1,2	5
4	To implement gate level multiplexers and MSI multiplexers	1,2	5
5	To design and implement MSI circuits of flip-flops	1,2	5
6	To design and implement mod 4 synchronous up/down counter using JK flip-flop	1,2	5
7	To configure MSI devices as asynchronous counter, synchronous counter as synchronous counters and universal shift register.	1,2	5
8	Mini-Project: Design and implement an application using digital circuit concepts.	1,2	5
Total Marks			40

References:

- [1] For datasheet refer: <http://www.datasheetcatalog.com>.
- [2] R. P. Jain and M. M. S. Anand, "Digital Electronics Practice Using Integrated Circuits," Tata McGraw Hill Education, 1983.