Course Code	Course Name	Teaching Scheme (Hrs/week)			Credits Assigned			
		L	T	P	L	T	P	Total
CE44	Computer Organization and Architecture	3	--	-	3	--	-	3
		Examination Scheme						
		Theory Marks						
		ISE		MSE		ESE		
		10		30		100 (60% Weight age)		

Pre-requisite Course Codes		CE32 (Digital Logic Design and Applications)
At the end of successful completion of this course, student will be able to		
Course Outcomes	CO1	To describe basic structure of computer
	CO2	To apply arithmetic algorithm for solving problems
	CO3	To demonstrate processor architectures with control signal generation.
	CO4	To describe the memory mapping techniques
	CO5	To apply I/O concept for simulating I/O device operations.
	CO6	To analyze different parallel processing and pipelining concepts

Module No.	Unit No.	Topics	Ref.	Hrs.
1		**Overview of Computer Architecture & Organization:**		
	1.1	Introduction of Computer Organization and Architecture, Basic organization of computer and block level description of the functional units,Evolution of x86 Computers, Von Neumann model, Harvard Model, Embedded system, ARM architecture	1,4	4
	1.2	Performance Issues: Designing for performance, Multicore, Mics, GPGPU.	1,4	2
2		**Data Representation and Arithmetic Algorithms:**		
	2.1	Number representation: Floating-point representation, Floating point arithmetic, IEEE 754 floating point number representation	5,7	2
	2.2	Integer Data computation: Addition, Subtraction. Multiplication: Signed multiplication, Booth's algorithm.	5,7	2
	2.3	Division of integers: Restoring and non-restoring division	5,7	2
3		**Processor Organization and Control Unit:**		
	3.1	CPU Architecture, Register Organization , ISA categories : Complex Instruction Set Computing ISA Features, Reduced Instruction Set Computing ISA Features. Instruction formats, basic instruction cycle. Instruction interpretation and sequencing,	2,4,6	4
	3.2	Control Unit :Soft wired (Micro-programmed) and hardwired	2,3	4

		control unit design methods. Microinstruction sequencing and execution. Micro operations, concepts of nano programming.		
	3.3	RISC and CISC: Introduction to RISC and CISC architectures and design issues.	3	1
4		**Memory Organization:**		
	4.1	Introduction to Memory and Memory parameters. Classifications of primary and secondary memories. Types of RAM and ROM, Allocation policies, Memory hierarchy and characteristics.	3	3
	4.2	Cache memory: Concept, architecture (L1, L2, L3), mapping techniques. Cache Coherency, Interleaved and Associative memory.	2,3	4
	4.3	Virtual Memory: Concept, Segmentation and Paging, Page replacement policies. LRU,FIFO	4,5	4
5		**I/O Organization and Introduction to Parallel Processing:**		
	5.1	Buses: Types of Buses ,Bus Arbitration, BUS standards	5,7	3
	5.2	I/O Interface, I/O channels, I/O modules and IO processor, Types of data transfer techniques: Programmed I/O, Interrupt driven I/O and DMA.	2,5,7	4
	5.3	Introduction to parallel processing concepts ,Flynn's classifications ,pipeline processing ,Pipeline stages, Hazards	5	3
			Total	**42**

References:

[1] Carl Hamacher, Zvonko Vranesic and Safwat Zaky, "Computer Organization", Fifth Edition, Tata McGraw-Hill.

[2] John P. Hayes, "Computer Architecture and Organization", Third Edition.

[3] William Stallings, "Computer Organization and Architecture: Designing for Performance", Eighth Edition, Pearson.

[4] B. Govindarajulu, "Computer Architecture and Organization: Design Principles and Applications", Second Edition, Tata McGraw-Hill.

[5] Dr. M. Usha, T. S. Srikanth, "Computer System Architecture and Organization",First Edition, WileyIndia."Computer Organization" by ISRD Group, Tata McGraw-Hill.

[6] Ramesh Gaonkar ,"Microprocessor architecture ,Programming and application with 8085",5th Edition, Penram

[7] Nicholas P Carter Adapted by Raj Kamal" "Computer Architecture and Organization",Schaum's Outline ,2nd edition.,Tata McGraw Hill.