Sardar Patel Institute of Technology

Bhavan's Campus, Munshi Nagar, Andheri (West), Mumbai-400058-India
(Autonomous Institute Affiliated to University of Mumbai)

Course Code	Course Name	Teaching Scheme (Hrs/week)			Credits Assigned			
		L	T	P	L	T	P	Total
EL33	Digital Circuits	3	1	--	3	1	--	4
		Examination Scheme						
		ISE		MSE	ESE			
		10		30	100 (60% Weightage)			

Pre-requisite Course Codes		ES21 (Basic Electrical Technology)
After successful completion of the course, student will be able to		
Course Outcomes	CO1	Explain various logic gates, SOP, POS forms and their minimization with k-map for given combinational circuits.
	CO2	Construct combinational circuits using given MSI devices.
	CO3	Discuss different types of programmable logic devices like PAL, PLA, CPLD and FPGA.
	CO4	Apply the knowledge of flip-flops and MSI to design sequential circuits
	CO5	Design state machines for given state diagrams after state reduction
	CO6	Discuss fault models and testing methods for digital circuits

Module No.	Unit No.	Topics	Ref.	Hrs.
1	1.1	**Logic Gates:** Basic gates, Universal gates, Sum of products and products of sum, minimization with Karnaugh Map (upto four variables), Quine Mc'Clusky method and realization.	1,2,3	12
	1.2	**Logic Families:** Types of logic families (TTL and CMOS), characteristic parameters (propagation delays, power dissipation, Noise Margin, Fan-out and Fan-in), transfer characteristics of TTL NAND, Interfacing CMOS to TTL and TTL to CMOS.	1,2,3	
	1.3	**Combinational Circuits using basic gates as well as MSI devices:** Half adder, Full adder, Half Subtractor, Full Subtractor, Multiplexer, Demultiplexer, Decoder, Comparator (Multiplexer and Demultiplexer gate level upto 4:1).	1,2,3	
2	2.1	**Sequential Logic:** Latches and Flip-Flops. Conversions of Flip-Flops, Timing Considerations and Metastability	1,2,3	12
	2.2	**Counters:** Asynchronous, Synchronous Counters, Up Down Counters, Mod Counters, Ring Counters Shift Registers, Universal Shift Register	1,2,3	

3	**3.1**	Mealy and Moore Machines, Clocked synchronous state machine analysis, State reduction techniques and state assignment, Clocked synchronous state machine design.	4,5	08
	3.2	MSI counters, MSI Shift registers and their applications	4,5	
4	**4.1**	Concepts of PAL and PLA. Introduction to CPLD and FPGA architectures.	4,5	05
5	**5.1**	Fault Models, Stuck at faults, Bridging faults, Controllability and Observability	6	05
	5.2	Path sensitization, ATPG, Design for Testability, Boundary Scan Logic, JTAG and Built in self test.	6	
			Total	**42**

References:

[1] William I. Fletcher, 'An Engineering Approach to Digital Design', PHI., First Edition

[2] R. P. Jain, "Modern Digital Electronics", Tata McGraw Hill, Forth Edition

[3] Morris Mano, "Digital Design", Pearson Education, Forth Edition

[4] John F. Wakerly, "Digital Design Principles And Practices, third Edition Updated, Pearson Education, Third Edition

[5] Stephen Brown and Zvonko Vranesic, "Fundamentals of digital logic design with VHDL", McGraw Hill, Second Edition.

[6] B. Holdsworth and R. C. Woods, "Digital Logic Design", Newnes, Forth Edition