Sardar Patel Institute of Technology

Bhavan's Campus, Munshi Nagar, Andheri (West), Mumbai-400058-India
(Autonomous Institute Affiliated to University of Mumbai)

Course Code	Course Name	Teaching Scheme (Hrs/week)			Credits Assigned			
		L	T	P	L	T	P	Total
ETL33	HDL Programming Lab	--	--	2	--	--	1	1
		Examination Scheme						
		ISE			ESE			Total
					Practical		Oral	
		40			10		10	60

Pre-requisite Course Codes		ET33 (Digital Circuits)
After successful completion of the course, student will be able to		
Course Outcomes	CO1	Write VHDL code to build the given hardware
	CO2	Verify the behavior of given hardware with VHDL simulation tool
	CO3	Write synthesizable VHDL code and perform physical verification on FPGA and CPLD device
	CO4	Write, simulate, synthesize and implement VHDL code with behavioral, dataflow and structural modeling style
	CO5	Interface the external peripherals with FPGA and design a hardware to create an application.
	CO6	Interpret the RTL, synthesis, Floorplan report and optimally utilize the internal resources of given FPGA

Exp. No.	Experiment Details	Ref.	Marks
1	Design, simulate and synthesize 9 bit parity generator using dataflow modeling and carry out physical verification on given FPGA.	1,2,3	5
2	Design, simulate and synthesize ripple carry adder and carry-look ahead adder using structural modeling and carry out physical verification on given FPGA	1,2,3	5

3	Design, simulate and synthesize a stepper motor control hardware using Johnson counter. Use behavioral modeling for designing this hardware. Carry out physical verification on given FPGA	1,2,3	**5**
4	Write the testbench to verify the given IP.	1,2,3	**5**
5	Interface ADC/ DAC with FPGA. Give input signal to ADC, digitally amplify the input signal, give amplified data to DAC and observe the amplified output on DSO.	1,2,3	**5**
6	FPGA implementation of Traffic light controller in VHDL using Finite State Machine	4	**5**
7	Design of Microcomputer using existing IP. Use instantiation for designing the hardware.	2	**5**
8	Mini project as an application of HDL	4	**5**
		Total Marks	**40**

References:

[1] J. Bhaskar, "VHDL Primer", Pearson Education.

[2] Gaganpreet Kaur, "VHDL Basic to Programming", Pearson

[3] Douglas Perry, "VHDL: Programming by Example" McGraw Hill

[4] Application notes by Xilinx and Altera