Sardar Patel Institute of Technology

Bhavan's Campus, Munshi Nagar, Andheri (West), Mumbai-400058-India
(Autonomous Institute Affiliated to University of Mumbai)

Course Code	Course Name	Teaching Scheme (Hrs/week)			Credits Assigned			
		L	T	P	L	T	P	Total
IT32	Digital Logic Design and Analysis	3	--	--	3	--	--	3
		Examination Scheme						
		ISE		MSE		ESE		
		10		30		100 (60%weightage)		

Pre-requisite Course Codes		ES11 (Basic Electrical and Electronics Engineering)
After successful completion of the course, student will be able to:		
Course Outcomes	CO1	Design of digital circuits using SOP &POS forms.
	CO2	Construct combinational circuits using given MSI devices.
	CO3	Apply the knowledge of flip-flops and MSI to design counters and Shift registers.
	CO4	Design state machines for given state diagrams after state reduction.
	CO5	Describe different types of programmable logic devices like PAL, PLA, CPLD and FPGA.

Module No.	Unit No.	Topics	Ref.	Hrs.
1	1.1	**Introduction to Number System & Digital Logic:** Introduction to Number System, Basic gates, Universal gates, Sum of products and products of sum, minimization with Karnaugh Map (up to four variables) and realization. Quine Mccluskey method.	1,2,3	16
	1.2	**Logic Families:** Types of logic families (TTL and CMOS), characteristic parameters (propagation delays, power dissipation, Noise Margin, Fan-out and Fan-in), transfer characteristics of TTL NAND, Interfacing CMOS to TTL and TTL to CMOS.	1,2,3	
	1.3	**Combinational Circuits using basic gates as well as MSI devices:** Half adder, Full adder, Half Subtractor, Full Subtractor, Multiplexer, De-multiplexer, Decoder, Comparator (Multiplexer and De-multiplexer gate level up to 4:1).	1,2,3	
2	2.1	**Sequential Logic:** Latches and Flip-Flops. Conversions of Flip-Flops, Timing Considerations and Metastability	1,2,3,4	05
3	3.1	**Counters:** Asynchronous, Synchronous Counters, Up Down Counters, Mod Counters.	1,2,4,5	11

	3.2	Mealy and Moore Machines, Clocked synchronous state machine analysis, State reduction techniques and state assignment, Clocked synchronous state machine design.	1,24,5	
	3.3	MSI counters and applications.	1,2,4,5	
4	**4.1**	**Shift Registers:** Shift Registers, Ring Counters, Universal Shift Register, MSI Shift registers and their applications.	1,2,4,5	05
5	**5.1**	**Programming Logic Devices:** Concepts of Programmable Array Logic (PAL) and Programming Logic Array (PLA).	1,2,4,5	05
	5.2	Introduction to Complex Programmable Logic Device (CPLD) and Field Programmable Gate Array (FPGA) architectures.	1,2,4,5	
			Total	**42**

References:

1. R. P. Jain, "*Modern Digital Electronics*", 4th Edition, Tata McGraw Hill, 2009.
2. Morris Mano, "*Digital Design",* 5th edition, Pearson Education, 2013.
3. William I. Fletcher, "*An Engineering Approach to Digital Design*", 1st Edition, PHI, 2009.
4. John F. Wakerley, "*Digital Design Principles And Practices*", 3rd Edition Updated, Pearson Education, Singapore, 2002
5. B. Holdsworth and R. C. Woods, "*Digital Logic Design*", 4thEdition, Newnes, 2002.