Sardar Patel Institute of Technology

Bhavan's Campus, Munshi Nagar, Andheri (West), Mumbai-400058-India
(Autonomous Institute Affiliated to University of Mumbai)

Course Code	Course Name	Teaching Scheme (Hrs/week)			Credits Assigned			
		L	T	P	L	T	P	Total
CPC501	**Microprocessor**	4	-	--	4	-	--	4
		Examination Scheme						
		ISE		MSE	ESE			
		10		30	100 (60% Weightage)			

Pre-requisite Course Codes	-	
At end of successful completion of this course, student will be able to		
Course Outcomes	CO1	Create assembly language and mixed language programs for 8086 based system.
	CO2	Design system using memory chips and peripheral chips for 8086 microprocessor.
	CO3	Illustrate techniques to improve performance of microprocessors.
	CO4	Distinguish between RISC and CISC.

Module No.	Topics	Ref.	Hrs.
1	**Intel 8086/8088 Architecture** 8086/8088 Microprocessor Architecture, Pin Configuration, Programming Model, Memory Segmentation, Study of 8284Clock Generator, Operating Modes, Study of 8288 BusController, Timing diagrams for Read and Write operations,Interrupts.	1-13	**10**
2	**Instruction Set and Programming** Instruction Set of 8086, Addressing Modes, AssemblyLanguage Programming, Mixed Language Programming with C Language and Assembly Language.	1-13	**8**
3	**System designing with 8086** Memory Interfacing: SRAM, ROM and DRAM (usingDRAM Controller-Intel 8203).Applications of the Peripheral Controllers namely 8255-PPI, 8253-PIT, 8259-PIC and 8237-DMAC. Interfacing of theabove Peripheral Controllers with 8086 microprocessor.3.3 Introduction to 8087 Math Coprocessor and 8089 I/OProcessor.	1-13	**12**
4	**Intel 80386DX Processor**	1-13	**6**

	Study of Block Diagram, Signal Interfaces, Bus Cycles,Programming Model, Operating Modes, Address TranslationMechanism in Protected Mode, Memory Management,Protection Mechanism.		
5	**Pentium Processor** Block Diagram, Superscalar Operation, Integer & FloatingPoint Pipeline Stages, Branch Prediction, CacheOrganization. Comparison of Pentium 2, Pentium 3 and Pentium 4Processors. Comparative study of Multi core Processors i3,i5 and i7.	1-13	**8**
6	**Super SPARC Architecture** SuperSPARC Processor, Data Formats, Registers, Memory model. Study of SuperSPARC Architecture.	1-13	**4**
		Total	**48**

References:

[1] Douglas Hall,"Microprocessor and Interfacing" Tata McGraw Hill.

[2] Liu & Gibson,"Microcomputer Systems: 8086/8088 family Architecture, Programming and Design". PHI Publication.

[3] Tom Shanley & Don Anderson,"Pentium Processor System Architecture", Addison-Wesley.

[4] Daniel Tabak,"Advanced Microprocessor", Tata McGraw Hill.

[5] Walter A Triebel,"The 80386DX Microprocessor: Hardware, Software and Interfacing", Prentice Hall.

[6] John Uffenbeck ,"8086/8088 family: Design Programming and Interfacing", PHI.

[7] Barry B. Brey,"Intel Microprocessors", Pearson Education India,8th Edition.

[8] Swati Joshi, Atul Joshi, Hemlata Jadhav,"Processor Architecture and Interfacing", Wiley.

[9] Das Lyla B, "The X86 Microprocessors: Architecture and Programming (8086 to Pentium)", Pearson Education India.

[10] The SPARC Architecture Manual

[11] I Intel Manuals

[12] Steven Armbrust, Ted Forgeron,"Programmer's Reference Manual for IBM Personal Computers", McGraw Hill

[13] Peter Abel,"IBM PC Assembly Language and Programming", Prentice Hall of India, 5th Edition.