



# Sardar Patel Institute of Technology

Bhavan's Campus, Munshi Nagar, Andheri (West), Mumbai-400058-India  
(Autonomous Institute Affiliated to University of Mumbai)

Course Code	Course Name	Teaching Scheme (Hrs/week)			Credits Assigned			
		L	T	P	L	T	P	Total
EXC601	Basic VLSI Design	4	--	--	4	--	--	4
		Examination Scheme						
		ISE		MSE		ESE		
		10		30		100 (60% Weightage)		

<b>Pre-requisite Course Codes</b>	EXC302: Electronic Devices EXC303: Digital Circuits and Design EXC402: Discrete Electronic Circuits EXC502: Design With Linear Integrated Circuits
After successful completion of the course, student will be able to	
<b>Course Outcomes</b>	CO1 Distinguish between technologies and MOSFET models
	CO2 Analyze MOSFET based circuits like inverters, logic circuits and semiconductor memories
	CO3 Design MOSFET based logic circuits with different design styles
	CO4 Design data path for adders, multipliers and shifters
	CO5 Discuss issues in VLSI Clocking and System Design

Module No.	Unit No.	Topics	Ref.	Hrs.
1		<b>Technology Trend</b>		06
	1.1	<b>Technology Comparison:</b> Comparison of BJT, NMOS and CMOS technology	1	
	1.2	<b>MOSFET Scaling:</b> Types of scaling, Level 1 and Level 2 MOSFET Models, MOSFET capacitances	1	
2		<b>MOSFET Inverters</b>		10
	2.1	<b>Circuit Analysis:</b> Static and dynamic analysis (Noise, propagation delay and power dissipation) of resistive load and CMOS inverter, comparison of all types of MOS inverters, design of CMOS inverters, CMOS Latch-up	1	
	2.2	<b>Logic Circuit Design:</b> Analysis and design of 2-I/P NAND and NOR using equivalent CMOS inverter	1	
3		<b>MOS Circuit Design Styles</b>		10
	3.1	<b>Design Styles:</b> Static CMOS, pass transistor logic, transmission gate, Pseudo NMOS, Domino, NORA, Zipper, C <sub>2</sub> MOS, sizing using logical effort	1,7	
	3.2	<b>Circuit Realization:</b> SR Latch, JK FF, D FF, 1 Bit Shift Register, MUX, decoder using above design styles	1,7	
4		<b>Semiconductor Memories</b>		08
	4.1	<b>SRAM:</b> ROM Array, SRAM (operation, design strategy, leakage currents, read/write circuits), DRAM (Operation 3T, 1T, operation modes, leakage currents, refresh operation, Input-Output circuits),	1,2	



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		Flash (mechanism, NOR flash, NAND flash)		
	<b>4.2</b>	<b>Peripheral Circuits:</b> Sense amplifier, decoder	1,2,3	
<b>5</b>		<b>Data Path Design</b>		<b>08</b>
	<b>5.1</b>	<b>Adder:</b> Bit adder circuits, ripple carry adder, CLA adder	7	
	<b>5.2</b>	<b>Multipliers and shifter:</b> Partial-product generation, partial-product accumulation, final addition, barrel shifter	7	
<b>6</b>		<b>VLSI Clocking and System Design</b>		<b>10</b>
	<b>6.1</b>	<b>Clocking:</b> CMOS clocking styles, Clock generation, stabilization and distribution	2,5,6	
	<b>6.2</b>	<b>Low Power CMOS Circuits:</b> Various components of power dissipation in CMOS, Limits on low power design, low power design through voltage scaling	5,6	
	<b>6.3</b>	<b>IO pads and Power Distribution:</b> ESD protection, input circuits, output circuits, simultaneous switching noise, power distribution scheme	5,6	
	<b>6.4</b>	<b>Interconnect:</b> Interconnect delay model, interconnect scaling and crosstalk	5,6	
			<b>Total</b>	<b>52</b>

## References:

- [1] Sung-Mo Kang and Yusuf Leblebici, "CMOS Digital Integrated Circuits Analysis and Design", Tata McGraw Hill, Third Edition.
- [2] Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic, "Digital Integrated Circuits: A Design Perspective", Pearson Education, Second Edition.
- [3] Etienne Sicard and Sonia Delmas Bendhia, "Basics of CMOS Cell Design", Tata McGraw Hill, First Edition.
- [4] Neil H. E. Weste, David Harris and Ayan Banerjee, "CMOS VLSI Design: A Circuits and Systems Perspective", Pearson Education, Third Edition.
- [5] Debaprasad Das, "VLSI Design", Oxford, First Edition.
- [6] Kaushik Roy and Sharat C. Prasad, "Low-Power CMOS VLSI Circuit Design", Wiley, Student Edition.
- [7] John P. Uyemura, "Introduction to VLSI Circuits and Systems", Wiley, Student Edition, 2013.