Sardar Patel Institute of Technology

Bhavan's Campus, Munshi Nagar, Andheri (West), Mumbai-400058-India
(Autonomous Institute Affiliated to University of Mumbai)

Course Code	Course Name	Teaching Scheme (Hrs/week)			Credits Assigned			
		L	T	P	L	T	P	Total
EXC603	Computer Organization	4	--	--	4	--	--	--
		Examination Scheme						
		ISE		MSE		ESE		
		10		30		100 (60% Weightage)		

Pre-requisite Course Codes		
After successful completion of the course, student will be able to		
Course Outcomes	CO1	Outline the basic structure of a digital computer and illustrate the integer and floating point arithmetic.
	CO2	Design the control unit of a CPU using two approaches namely hardwired and micro-programmed control.
	CO3	Classify and Create a memory organization
	CO4	Discuss the concepts of I/O organization
	CO5	Discuss instruction level parallelism and IA32 family architecture.

Module No.	Unit No.	Topics	Ref.	Hrs.
1		**Introduction to Computer Organization**		10
	1.1	Fundamental units of computer organization, evolution of computers, von neumann model, performance measure of computer architecture	1,3	
	1.2	Introduction to buses and connecting I/O devices to CPU and Memory, bus structure,	1,3	
	1.3	Introduction to number representation methods, integer data computation, floating point arithmetic.	3	
2		**Processor Organization and Architecture**		14
	2.1	CPU Architecture, register organization, instruction formats, basic instruction cycle, instruction interpretation and sequencing	1,3	
	2.2	**Control unit:** soft wired (micro-programmed) and hardwired control unit design methods	1,3	
	2.3	Microinstruction sequencing and execution, micro operations, concepts of nano programming.	1,3	
	2.4	Introduction to RISC and CISC architectures and design issues, case study on 8085 microprocessor, features, architecture, pin configuration and addressing modes		
3		**Memory Organization**		12
	3.1	Introduction to memory and memory parameters, classifications of primary and secondary memories, types of RAM and ROM, allocation policies, memory hierarchy and characteristics	1,3	
	3.2	Cache memory concept, architecture (L1, L2, L3), mapping techniques, cache coherency	1,3	
	3.3	Interleaved and associative memory, virtual memory, concept,	1,3	

		segmentation and paging, page replacement policies		
4		**Input / Output Organization**		**08**
	4.1	Types of I/O devices and access methods, types of buses and bus arbitration, I/O interface, serial and parallel ports	1,3	
	4.2	Types of data transfer techniques, programmed I/O, interrupt driven I/O and DMA	1,3	
	4.3	Introduction to peripheral devices, scanner, plotter, joysticks, touch pad, storage devices	1,3	
5		**Introduction To Parallel Processing System**		**04**
	5.1	Introduction to parallel processing concepts, Flynn" s classifications, pipeline processing, instruction pipelining, pipeline stages, pipeline hazards	1,2	
6		**Introduction to Intel IA32 Architecture**.		**04**
	6.1	Intel IA32 family architecture, register structure, addressing modes, advancements in arithmetic and logical instructions, exception handling in IA32 architecture	1	
			Total	**52**

References:

[1] Carl Hamacher, Zvonko Vranesic and Safwat Zaky, "Computer Organization", Tata McGraw-Hill, Fifth Edition

[2] John P. Hayes, "Computer Architecture and Organization", Third Edition.

[3] William Stallings, "Computer Organization and Architecture: Designing for Performance", Pearson, Eighth Edition.

[4] B. Govindarajulu, "Computer Architecture and Organization: Design Principles and Applications", Tata McGraw-Hill, Second Edition.

[5] Dr. M. Usha and T. S. Srikanth, "Computer System Architecture and Organization", Wiley-India, First Edition.

[6] Ramesh Gaonkar, "Microprocessor Architecture, Programming and Applications with the 8085", Penram, Fifth Edition.