Sardar Patel Institute of Technology

Bhavan's Campus, Munshi Nagar, Andheri (West), Mumbai-400058-India
(Autonomous Institute Affiliated to University of Mumbai)

Course Code	Course Name	Teaching Scheme (Hrs/week)			Credits Assigned			
		L	T	P	L	T	P	Total
EXL601	VLSI Design Laboratory	--	--	2	--	--	1	1
		Examination Scheme						
		ISE		ESE			Total	
				Practical		Oral		
		40		--		20		60

Pre-requisite Course Codes		
After successful completion of the course, student will be able to		
Course Outcomes	CO1	Make use of simulation tools to verify characteristics of MOSFET based circuits
	CO2	Set-up simulation environment for VLSI circuit simulation
	CO3	Observe characteristics of MOSFETS via simulation
	CO4	Discuss tradeoffs in VLSI circuits by observing simulation results
	CO5	Validate design of MOSFET based circuits
	CO6	Reproduce the given abstract of the IEEE paper

Exp. No.	Experiment Details	Ref.	Marks
1	To Analyze NMOS and PMOS Transistor characteristics.	1,2	5
2	To simulate Resistive Load Inverter and CMOS Inverter, verify the VTC. Compare both the topologies. Comment on the Noise Margins.	1,2	5
3	Implement CMOS NAND, NOR, AND, OR using Static CMOS Logic.	1,2	5
4	Design and Implement AB+CD bar using different CMOS Logic styles.	1,2	5
5	Simulate Pseudo NMOS Inverter and comment on the result.	1,2	5
6	Simulate 6 Transistor SRAM and check the read and write stability	1,2	5
7	Design and Implement given equation using Pseudo NMOS ,Domino Logic and C^2MOS Logic	1,2	5
8	Simulate Clocked JK and D Flip Flop using Static CMOS Logic.	1,2	5
		Total Marks	40

References:

[1] Sung-Mo Kang and Yusuf Leblebici, "*CMOS Digital Integrated Circuits Analysis and Design*", Tata McGraw Hill, 3rd Edition.

[2] Etienne Sicard and Sonia Delmas Bendhia, "*Basics of CMOS Cell Design*", Tata McGraw Hill, First Edition.