Sardar Patel Institute of Technology

Bhavan's Campus, Munshi Nagar, Andheri (West), Mumbai-400058-India
(Autonomous Institute Affiliated to University of Mumbai)

Course Code	Course Name	Teaching Scheme (Hrs/week)			Credits Assigned			
		L	T	P	L	T	P	Total
ETC606	VLSI Design	4	-	--	4	-	--	4
		Examination Scheme						
		ISE		MSE		ESE		
		10		30		100 (60% Weightage)		

Pre-requisite Course Codes	ETC303: Digital Electronics ETC302: Analog Electronics-I ETC402: Analog Electronics-II ETC505: Integrated Circuits
After successful completion of the course, student will be able to	
Course Outcomes	CO1 To evaluate MOSFET fabrication techniques and scaling
	CO2 To evaluate DC and transient analysis of CMOS logic.
	CO3 To illustrate MOS circuit design styles.
	CO4 To evaluate Semiconductor memories.
	CO5 To illustrate Data path design.
	CO6 To illustrate VLSI clocking and system design

Module No.	Unit No.	Topics	Ref.	Hrs.
1	**MOSFET Fabrication and Scaling**		3,5	08
	1.1	**Fabrication:** Fabrication process flow for NMOS and CMOS, CMOS Latch-up		
	1.2	**MOSFET Scaling:** Types of scaling, short channel effects, Level 1 and Level 2 MOSFET Models		
	1.3	**Layout:** Lambda based design rules, MOSFET capacitances		
2	**MOSFET Inverters**		1,3,5	10
	2.1	**Circuit Analysis:** Static and dynamic analysis (Noise, propagation delay and power dissipation) of resistive load and CMOS inverter. Comparison of all types of MOS inverters. Design of CMOS inverters and its layout.		
	2.2	**Logic Circuit Design:** Analysis and design of 2-I/P NAND and NOR using equivalent CMOS inverter.		
3	**MOS Circuit Design Styles**		3,5	10
	3.1	**Design Styles:** Static CMOS, Pass Transistor Logic, Transmission Gate, Pseudo NMOS, Domino, NORA, Zipper, C^2MOS		
	3.2	**Circuit Realization:** SR Latch, JK FF, D FF, 1 Bit Shift Register, MUX, Decoder using above design styles and their layouts		
4	**Semiconductor Memories**		2,4	08

	4.1	**SRAM:** ROM Array, SRAM (operation, design strategy, leakage currents, read/write circuits), DRAM (Operation 3T, 1T, operation modes, leakage currents, refresh operation, Input-Output circuits), Flash (mechanism, NOR flash, NAND flash), layout of SRAM and DRAM		
	4.2	**Peripheral Circuits:** Sense Amplifier, Decode		
5	**Data Path Design**		3,4,5	08
	5.1	**Adder:** Bit adder circuits, Ripple carry adder, CLA adder		
	5.2	**Multipliers and shifter:** Partial-product generation, partial-product accumulation, final addition, Barrel Shifter		
6	**VLSI Clocking and System des**		3,5	08
	6.1	**Clocking:** CMOS clocking styles, Clock generation, stabilization and distribution.		
	6.2	**Low Power CMOS Circuits:** Various components of power dissipation in CMOS, Limits on low power design, low power design through voltage scaling.		
	6.3	**IO pads and Power Distribution:** ESD protection, Input circuits, Output circuits, Simultaneous switching noise, power distribution scheme		
	6.4	**Interconnect:** Interconnect delay model, interconnect scaling and crosstalk.		
			Total	**52**

References

1. Sung-Mo Kang and Yusuf Leblebici, "*CMOS Digital Integrated Circuits Analysis and Design*", Tata McGraw Hill, 3rd Edition, 2012.
2. Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic, "*Digital Integrated Circuits: A Design Perspective*", Pearson Education, 2nd Edition.
3. John P. Uyemura, "*Introduction to VLSI Circuits and Systems*", Wiley, Student Edition, 2013.
4. Neil H. E. Weste, David Harris and Ayan Banerjee, "*CMOS VLSI Design: A Circuits and Systems Perspective*", Pearson Education, 3rd Edition.
5. R. Jacob Baker, "*CMOS Circuit Design, Layout and Simulation*", Wiley, 2nd Edition, 2013