[REVISED COURSE]

CON/5083-05. PR-7400

(3 Hours) [Total Marks : 100

1) Question No. 1 is compulsory.
2) Attempt any four out of remaining six questions,
3) Assume suitable data wherever required.
4) Figures to the right indicate full marks.
5) Illustrate answers with sketches wherever require

1\. A) Realize the following function using CMOS logic. F = (A+B+C).D Also draw the stick diagram for the same. (03)

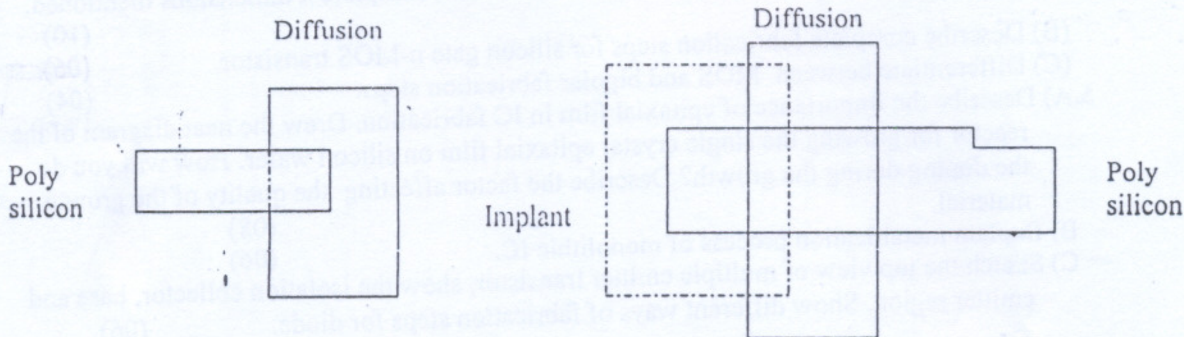
B) Draw the pass transistor logic based 4:1 multiplexer. Also draw the standard cell required for mux design, mention the cell λ dimensions. (03)

C) Show complete layout representation for all possible contact types between polysilicon to metal, diffusion to metal, metal to metal and polysilicon todiffusion. (03)

D) Differentiate butting contact, buried contact and respective conventional contact through metal with respect to cross sectional view, processing step required and reliability. (04)

E) Discuss fabrication density, system speed, power dissipation and their interdependence in detail. (03)

F) For the diagram given below, suggest which type of the errors will occur while working on layout editor. (02)



G) If some layout editor defines minimum diffusion width of 4λ , poly-silicon width of 2λ then draw the layout for transistor having aspect ratio of 1:2. (02)

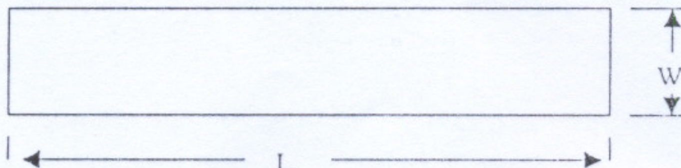
2\. (A) Discuss the following terms in detail (08)
a) Early effect voltage with respect to short channel effect.
b) Mobility saturation and thermal variation.
c) Calculation of source and drain capacitances of area A and perimeter P.
d) Fermi level, work function difference and strong surface inversion.

(B) Draw in detail the cross sectional view of FET capacitances. Derive the expression for total capacitance of source and drain region of area A and perimeter P. (08)

(C) Describe different modes of operation of MOSFET with the help of cross sectional view, (04)

3\. (A) Following table gives the area capacitance values for MOS circuits find out □Cg capacitance for 5μ, 2 μ, and 1.2 μ technologies. (08)

If the following geometry gives the length to width ratio of (a) metal1 (2) polysilicon and (c) n type diffusion then calculate the capacitance values for metal1 to substrate, polysilicon to substrate and n type diffusion to substrate.



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Capacitance	Value in $pf \times 10^{-4} / \mu m^2$		
	5 µm	2 µm	1.2 µm
Gate to channel	4	8	16
Diffusion	1	1.75	3.75
Poly to Substrate	0.4	0.6	0.6
Metal1 to Substrate	0.3	0.33	0.33

3.(B) Typical sheet resistance Rs for MOS layers for 5 micron technology is given as (08)

Layer	Rs Ω/□
Metal	0.03
Diffusion	10-50
Silicide	2-4
Polysilicon	15-100
n- transistor channel	10^4
p- transistor channel	2.5×10^4

Calculate the ON resistance for the following n-MOS inverter with Rinv = 4, Zp.u = 1:1 and for CMOS inverter with Zp.d =1:1 (08)

(C) Discuss the operation of NMOS transistor both for enhancement and depletion type with the help of (Vds Vs Ids) and (Vgs Vs Ids) characteristics. (04)

4.(A) Draw stick layout for NMOS two input NAND gate with depletion MOSFET as the load with aspect ratio of 4:1, also draw layout with complete λ dimensions mentioned. (10)

(B) Describe complete fabrication steps for silicon gate n-MOS transistor. (06)

(C) Differentiate between MOS and bipolar fabrication steps. (04)

5.A) Describe the importance of epitaxial film in IC fabrication. Draw the neat diagram of the reactor for growing the single crystal epitaxial film on silicon wafer. How will you do the doping during the growth? Describe the factor affecting the quality of the growth material. (08)

B) Explain metallization process of monolithic IC. (06)

C) Sketch the top view of multiple emitter transistor, show the isolation collector, base and emitter region. Show different ways of fabrication steps for diode. (06)

6.A) Explain the following :– (10)

1) Importance of substrate biasing.
2) Importance of buried layer.
3) Schottky barrier and ohmic contact in BJT fabrication.
4) Growth of n^+ layer for collector contact in BJT fabrication.
5) Thin film resistor fabrication and trimming.

B) A base diffusion layer length is 100 micro meter and it's width is 10 micro meter. The sheet resistance of the layer is 100 ohm/sq. Calculate it's resistance. (05)

C) What is the minimum number of isolation region is required to realize TTL NAND gate ? (05)

7. Write note on :– (20)

a) Lateral PNP and vertical PNP transistor.
b) n-well process steps and cross sectional view.
c) Rise time of EMD pull up inverter.
d) IC cross over
e) Ion implantation and diffusion process