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Cmptr Organisation Architecture

28/11/06

S.E. (Cmptr) Sem. IV (Rev)

YM-5437

IT

(REVISED COURSE)

(3 Hours)

[Total Marks : 100

- N.B.** (1) Question No. 1 is **compulsory**.
(2) Attempt any **four** out of remaining questions.
(3) Figures to the **right** indicate **full** marks.
1. (a) Explain structure of computer define by Sir Von Neumann. 8
(b) Explain different addressing mode with example (atleast 6). 12
 2. (a) Explain the characteristics of RISC & CISC. 10
(b) Explain the different Raid Level. 10
 3. (a) Explain with necessary flow chart— 8
(i) Programmed I/o (ii) Interrupt driven I/o.
(b) Explain element of cache design in brief w.r.t. (Cache size, mapping, write policy etc). 12
 4. (a) Explain with help of functional diagram Microprogrammed Control Unit. 10
(b) Explain Flynn's classification for parallel processing system. 10
 5. (a) Explain the six stage instruction pipeline with necessary diagram. 10
(b) Write the algorithm for floating point addition. 10
 6. (a) Explain the different element considered while design the Bus interconnection architecture. 12
(b) Explain Asynchronous ALU. 8
 7. Write short notes on (any **four**) :- 20
 - (a) PCI BUS.
 - (b) Synchronous ALU
 - (c) Demanded paging.
 - (d) Page segmentation.
 - (e) IEE Y54 STD.