

Digital Design

YM-5416

Nov. 1 Pr. 99  
Con. 4700-06.

(REVISED COURSE)

(3 Hours)

[ Total Marks : 100

23/6/2008

- N.B. (1) Question No. 1 is compulsory.  
(2) Attempt any four out of remaining six questions.

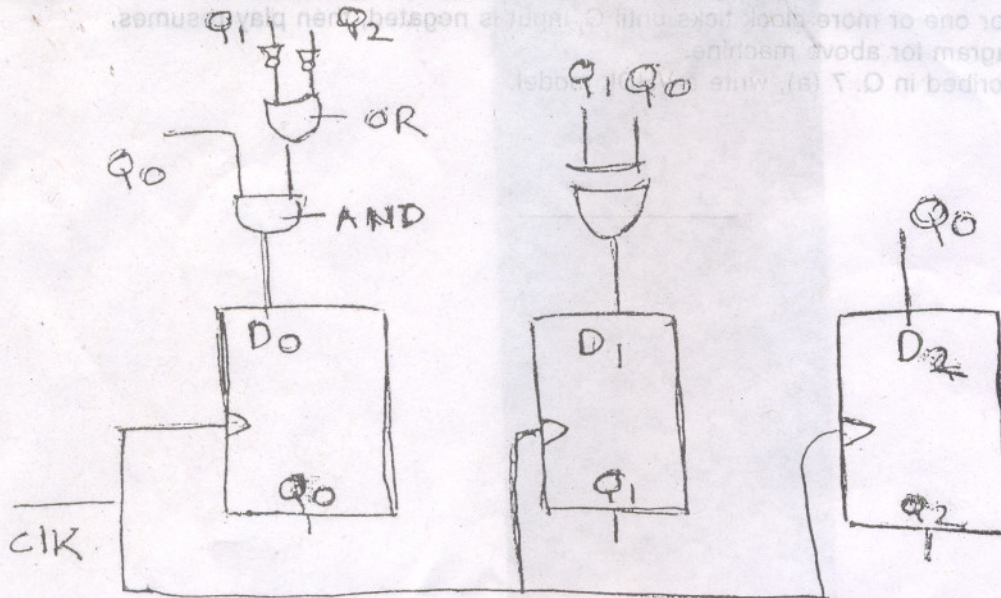
1. Attempt all questions of 5 marks each :-

- (a) Develop excitation table for non-standard GL Flipflop defined by following characteristic equation—  
$$Q_{n+1} = G \bar{Q}_n + LQ_n$$
  
(b) Design 3 bit asynchronous up/down counter using JK Flipflops.  
(c) Develop state diagram for serial binary adder to be designed as Mealy machine.  
(d) Develop state diagram for serial binary adder to be designed as Moore machine.

20

2. (a) Analyze sequential machine shown and develop its state diagram—

10



(b) Redesign above machine using MN Flipflop having characteristic table as—

10

M	N	$Q_{n+1}$
0	0	0
0	1	$Q_n$
1	0	$Q_n$
1	1	1

3. (a) Design MOD 10 (Decade) synchronous counter using JK Flipflops. Use Minimal Risk approach of designing. 10  
(b) Redesign above counter using minimal cost approach. Comment on quantum of hardware saved with this approach. 10

4. (a) Discuss various modes of operating IC 7490. Also include sequence tables for various modes. **10**  
 (b) Apply Partitioning method and obtain minimize state diagram. **10**

X	0	1	
A	B	C	1
B	D	F	1
C	F	E	0
D	B	G	1
E	F	C	0
F	E	D	0
G	F	G	0

Y o/p (Moore machine)

5. (a) Develop state table for single input, single output Mealy machine that is searching for two sequences 1010 and 0101. Both the sequences are overlapping. **10**  
 (b) Develop state table for above machine in Q (a), if it is to be designed as Moore machine. **10**

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6. (a) A sequential circuit has two inputs  $w_1$  and  $w_2$  and an out put  $z$ . Its function is to compare the input sequence on two inputs. If  $w_1 = w_2$  during any four consecutive clock cycles the circuit produces  $z = 1$  otherwise  $z = 0$ . Develop circuit as a Mealy machine. Use D Flipflops and decoders (for generation of excitation inputs). 10
- (b) Write short note on (any one) – 10
- (i) Xilinx XC 9500 CPLD family.
  - (ii) Estimation of Digital System Reliability.
7. (a) Design clocked synchronous state machine with four inputs  $G_1 - G_4$  that are connected to push buttons. The machine has four outputs  $L_1 - L_4$  connected to Lamps located near the like numbered push-button. There is also an ERR output connected to a Red Lamp. In normal operation  $L_1 - L_4$  outputs display a 1 out of 4 pattern. At each clock tick, the pattern is rotated by one position. Guesses are made by pressing a push-button which asserts an input  $G_i$ . When any  $G_i$  input is asserted, the ERR outputs is asserted if the wrong push-button is pressed, that is, if  $G_i$  input detected at clock tick does not have the same number as the lamp output that was asserted before the clock tick. Once a guess has been made, play stops and ERR output maintains the same value for one or more clock ticks until  $G_i$  input is negated, then play resumes. Develop state diagram for above machine. 10
- (b) For machine described in Q. 7 (a), write a VHDL model. 10