T.E. Sem. V (Rev) - ExTC NOV. 06

Con. 4819-06. Elements of Microelectronics YM-6760

(REVISED COURSE)

(3 Hours) [Total Marks : 100

N.B. : (1) Question No. **1** is **compulsory**.
(2) Attempt any **four** of the remaining **six** questions.
(3) Assume **suitable data** wherever **necessary**.

1. (a) With the help of a neat diagram explain the important features of butting and buried contacts. 5
(b) Explain IC crossovers. 5
(c) List double metal MOS process rules. 5
(d) How does a "dummy collector" present Latching ? 5

2. (a) Discuss scaling factors for device parameters. 10
(b) Describe the formation of resistors in intergrated circuit. How will you optimize the design ? 10

3. (a) Discuss the parasitic effects in BJTS. 10
(b) Draw the stick diagram and a mask layout for an 8:1 nMOS inverter circuit both the input and output points should be on the polysilicon layer. 10

4. (a) With neat diagrams explain the fabrication sequence of CMOS inverter using the p-well process. 10
(b) Calculate the native threshold voltage for an n-transistor at 300°K for a process with a Si-substrate with $N_A = 1 \cdot 80 \times 10^{16}$, a SiO_2 gate oxide with thickness 200 A°. (Assume $\phi_{ms} = -0 \cdot 9$ V, $Q_{fc} = 0$) 10

5. (a) What is photolithography ? What are the different techniques involved in it ? Explain one of them in detail. 10
(b) Draw stick diagram and layout for nMOS shift register cell. 10

6. (a) In the inverter circuit, what is meant by $Z_{p.u.}$ and $Z_{p.d.}$? Derive the required ratio between $Z_{p.u.}$ and $Z_{p.d}$. it an nMOS inverter is to be driven from another nMOS inverter. 10
(b) What is epitaxy ? What are the different epitaxial processes ? Explain one of them in detail. 10

7. (a) What are the advantages of twin-tub process over n-well process ? 5
(b) Explain limitations of scaling. 5
(c) Explain ion-implantation technique. 5
(d) Explain significance of lambda-based design rules for MOS-IC. 5