

Con. 5290-07.

[REVISED COURSE]

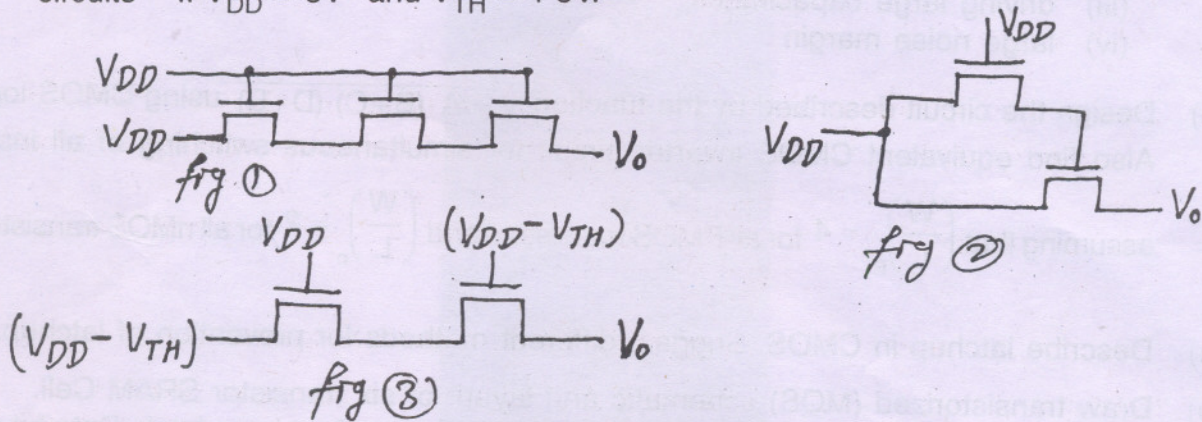
CD-7104

(3 Hours)

[Total Marks : 100

- N.B. : (1) Question No. 1 is compulsory.
 (2) Attempt any four questions out of remaining six questions.
 (3) Assume suitable data, wherever required.
 (4) Symbols have their usual meanings.

1. (a) Describe the effect of hot electron effect and short channel effect on the characteristics of MOSFET. 5
 (b) Draw and explain the profile for diffusion from – 5
 (i) Constant source
 (ii) Instantaneous source.
 Clearly indicate different diffusion times.
 (c) Describe physical, electrical and its corresponding logical fault model with an example. 5
 (d) In short, explain what is pass transition logic. Calculate the output voltage for following circuits – If $V_{DD} = 5V$ and $V_{TH} = 1.5V$. 5



2. (a) PMOS transistor was fabricated on n-type substrate with bulk doping density of $N_D = 10^{16} \text{ cm}^{-3}$, gate doping density (n-type poly) of $N_D = 10^{20} \text{ cm}^{-3}$, $\frac{Q_{ox}}{q} = 4 \times 10^{10} \text{ cm}^{-2}$ and oxide thickness of $t_{ox} = 0.1 \mu\text{m}$. Calculate the threshold voltage at room temperature for $V_{SB} = 0$. Use $\epsilon_{si} = 11.7 \epsilon_0$. 10
 (b) Draw the cross section for all the important masking steps required to fabricate n well CMOS inverter. 10
3. (a) Derive the following expression for CMOS inverter – 10

$$V_{IL} = \frac{2V_{out} + V_{TO,P} - V_{DD} + K_R V_{TO,n}}{(1 + K_R)}$$

$$V_{IH} = \frac{V_{DD} + V_{TO,P} + K_R (2V_{out} + V_{TO,n})}{(1 + K_R)}$$

Where $K_R = \frac{K_n}{K_p}$

- (b) Determine pull up to pull down ratio $\left(\frac{Z_{PU}}{Z_{PD}} \right)$ for an nMOS inverter driven by another nMOS inverter. 10

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4. (a) Explain any five limitations of scaling in detail. 10
- (b) Draw stick diagram and Mask layout using λ based design rules for three input NMOS E-D (enhancement-depletion) technology NAND gate. 10

The reference inverter has $\left(\frac{W}{L}\right)_{\text{load}} = \frac{1}{4}$

and $\left(\frac{W}{L}\right)_{\text{drivers}} = \frac{1}{2}$

5. (a) For each of the following, state whether CMOS or bipolar design styles are preferred. Why? 10
- low power dissipation
 - low delay time
 - driving large capacitance
 - large noise margin.
- (b) Design the circuit described by the function $y = \overline{A \cdot (B+C) \cdot (D+E)}$ using CMOS logic. Also find equivalent CMOS inverter circuit for simultaneous switching of all inputs assuming that $\left(\frac{W}{L}\right)_P = 4$ for all PMOS transistors and $\left(\frac{W}{L}\right)_n = 2$ for all nMOS transistors. 10
6. (a) Describe latchup in CMOS. Suggest different methods for prevention of latchup. 10
- (b) Draw transistorized (MOS) schematic and layout of six transistor SRAM Cell. [SRAM cell has back to back connected CMOS inverters forming a latch. Data bit and $\bar{\text{bit}}$ is given to this latch through access transistors which is controlled by word line WL. Access transistors are of nMOS type]. 10
7. Write detail note on any **four** :- 20
- Controllability and observability
 - Various types of pull up's used in MOS inverter circuits. (Draw only circuit diagrams, list their advantages and disadvantages, if any)
 - Design rules and their necessity
 - Buried and Butting contact
 - Ion implantation.