

M. E Sem I (Etox) (Map & system-I)
(Microprocessors - & system-I)

10/12/07

Con. 5483-07.

BB-7503

(3 Hours)

[Total Marks : 100

N.B (1) Question No. 1 is **compulsory**.(2) Attempt any **four** questions out of the remaining **six** questions.(3) Assume **suitable** data and state the assumptions **clearly**.

1. Design a single Board Computer with the following specifications : 20
 - (i) CPU-80386 DX operating at 25 MHz.
 - (ii) Firmware support of 128KB of EPROM using 32KB devices.
 - (iii) Data memory support of 512KB using 64KB SRAM devices.
 - (iv) 2 input and 2 output ports-all interrupt driven.

Draw a neat diagram, show memory and I/O maps and decoding logic used.
2. Explain what is TSS. Explain, with neat diagram, task switching mechanism of 80386DX (Direct and Indirect Switch). Give protection rules associated with it. 20
3. Explain the following Translation mechanism with neat Diagrams :— 20
 - (i) 48-bit Virtual address to 32-bit Linear address.
 - (ii) 32-bit Linear address to 32-bit Physical address.
4. Explain Trojan Horse Attack. How operating system can prevent such an attack using ARPL instruction ? 20
5. (a) Draw the interfacing diagram which consists of 80386 DX and 82385 DX. Explain. 10
(b) Explain Cache Coherency problem. Explain how 82385 DX determines Cache hit and Cache miss. 10
6. (a) Describe ISA bus cycle for 16-bit memory with timing diagram. 10
(b) Explain, with neat diagram, how ISA bus system can handle 32-bit memory operations. 10
7. Explain the architecture of 80386 EX with a proper diagram. Explain the function of configuration registers. 20