M.E. Sem II (Etox) VLSI Design 08/12/07

Con. 5432-07. BB- 7437

(3 Hours) [Total Marks : 100

N. B. : (1) Q. No. **1** is **compulsory.**
(2) Attempt any **four** out of remaining **six** questions.
(3) Assume any **suitable** data wherever required but justify the **same.**

1 a Define Inverter Ratio. and state its significance. 20

b What is burried contact? When we use this in MOS technology

c Compare between Silicon and Germanium Technology..

d Define Sheet Resistance, What is the significance of it?

e Draw the Exclusive OR using minimum devices in CMOS Technology?

2 a Implement following function also draw the stick diagram 10

$$F = \overline{X + (Y.Z)}$$

Draw Layout for the same.

b Using nMOS devices design 4:1 MUX also draw the stick diagram. 10

3 a Explain the effect of scaling on interconnect with respect to power dissipation and delay 10

b Describe with neat diagram various steps involved in fabrication and sketch each mask steps in cross-sectional view of wafer for nMOS device. 10

4 a Derive expression for nMOS transistor current in both regions of operations. 10

b Find the expression for Threshold voltage of pMOS device also explain the effect of substrate potential(Body Effect)on Threshold & overall performance of the device 10

5 a Explain following short channel effects: 10

i) Threshold voltage roll off
ii) Drain Punch-through
iii) Velocity saturation
iv) Hot carrier effect.

b Prepare a chart of CMOS Inverter characteristics in five different regions. Specify for the devices the region of operation and justify. 10

6 a Derive Noise margin for Resistive load type of an Inverter 10

b What is total power dissipation in case of CMOS Inverter? Discuss how to approximate the estimation of total power dissipation? What is power budget ? how to minimize the Power Dissipation? 10

7 Write short notes on: (any four) 20

a CMOS Domino Logic

b Explain MOS Capacitor and Band Bending in P-type of Semiconductor .

c Need & Effect of scaling.

d Latch-up problem in CMOS device

e Electron beam lithography

f Super buffer and its importance in IC design