Con. 5120-07. CD-5802

(REVISED COURSE)

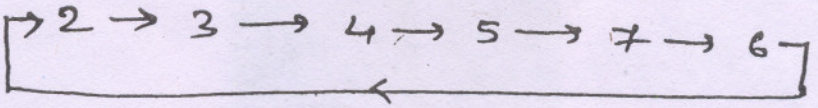
(3 Hours) [Total Marks : 100

N.B. (1) Question No. **1** is **compulsory.**
(2) Attempt any **four** out of remaining **six** questions.
(3) Figures to the **right** indicate **full** marks.

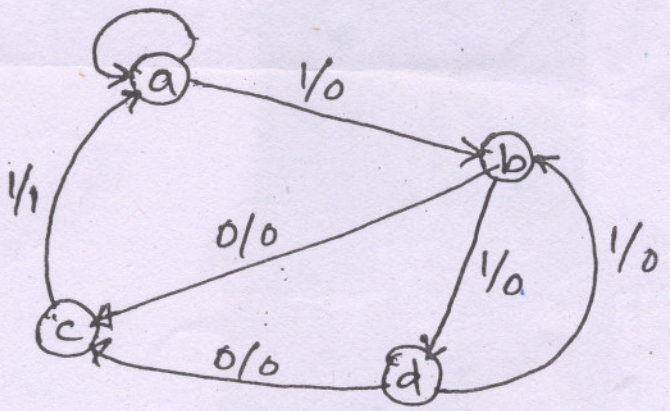
1. (a) Compare synchronous counters and asynchronous counters. 6
   (b) Draw a switch debouncer using NAND gates and explain it. 8
   (c) Develop state diagram for serial binary adder to be designed as Moore machine. 6

2. (a) Design a MOD-100 counter using IC-7493. 10
   (b) Design two bit Bidirectional shift register using JK flip-flop. Follow all the steps in designing of sequential machine. 10

3. (a) Design a synchronous counter with JK flip-flops which runs through a sequence of– 10



   (b) The sequential state diagram may have one or more redundant states. Using state reduction technique obtain the minimised state diagram. 10



4. (a) Write a VHDL code for a left to right shift register with an enable input. 10
   (b) Draw and explain logic diagram for 8 × 4 diode ROM. 10

5. (a) Design a state machine that detects three or more consecutive 1's in a string of bits coming through an input line. Synthesize the circuit using D flip-flops. 10
   (b) Write a VHDL code for a two digit BCD counter. 10

6. (a) Draw the universal state diagram for a 4-bit serial in parallel out right shift register. How twisted ring counter can be designed using this register ? 10
   (b) Discuss CPLD Xilinx XC 9500 architecture with neat block diagram. Describe main features. 10

7. Write a short notes on (any **two**) :– 20
   (a) XC 4000 FPGA family
   (b) VHDL features
   (c) Estimation of digital system reliability.