Con. 5013–07. CD–6084

(3 Hours) [Total Marks : 100

N.B. : (1) Question No. **1** is **compulsory**.
(2) Attempt any **four** questions out of remaining **six** questions.

1. (a) How does a "dummy collector" present Latching ? **5**
(b) Explain limitations of scaling. **5**
(c) Define LSI, MSI and VLSI circuits. **5**
(d) Explain ion-implantation technique. **5**

2. (a) (i) What is the stored charge and the number of electrons on an MOS capacitor with an area of 4 μm^2, a dielectric of 200 °A thick SiO_2 and an applied voltage of 5V ? **6**
(ii) Explain IC crossovers. **4**
(b) Discuss scaling factors for device parameters. **10**

3. (a) Explain the need of design rules and explain significance of λ-based design rules. **10**
(b) Draw the stick diagram and a mask layout for an 8 : 1 nMOS inverter circuit both the input and output points should be on the polysilicon layer. **10**

4. (a) With neat diagrams explain the lubrication sequence of CMOS inverter using the n-well process. **10**
(b) What is the minimum number of isolation regions required to realize in monolithic form for 2 input TTL NAND gate. Draw monolithic layout of this gate. **10**

5. (a) What is epitaxy ? What are the different epitaxial processes ? Explain one of them in detail. **10**
(b) Design CMOS logic gates for the following functions :– **10**
(i) $z = \overline{A \cdot B \cdot C \cdot D}$
(ii) $z = \overline{A \cdot (B + D) + C}$

6. (a) In the inverter circuit, what is meant by Zp.u. and Zp.d. ? Derive the required ratio between Zp.u. and Zp.d. if an nMOS inverter is to be driven from another nMOS inverter. **10**
(b) Describe the formation of resistors in integrated circuit. How will you optimize the design ? **10**

7. Write short note on the following :–
(a) Double Metal MOS Process Rules **5**
(b) Butting and Buried Contacts **5**
(c) Lateral PNP and Vertical PNP Transistor **5**
(d) Rise time of EMD pull-up Inverter. **5**