

Con. 5711-08.

RC-7244

(REVISED COURSE)

(3 Hours)

[Total Marks : 100]

- N.B. :** (1) Question No.1 is **compulsory**.
 (2) Attempt any **four** questions out of remaining **six** questions.
 (3) Assume **suitable data** wherever **necessary** and state **clearly**.

1. (a) Compare Resistive load, Depletion load and Enhancement load 10
inverters. Also write their merits, demerits and applications.
- (b) Explain the operation of CMOS inverter with clearly mentioning the 10
five cases given below :—
 - (i) $V_{in} < V_{TO,n}$
 - (ii) $V_{in} = V_{IL}$
 - (iii) $V_{in} = V_{IH}$
 - (iv) $V_{in} > V_{DD} + V_{TO,p}$
 - (v) $V_{in} = V_{TH}$ (Inverter Threshold).
2. (a) For the CMOS inverter, let the supply voltage $V_{DD} = 1.8V$, the threshold 10
voltage for both NMOS and PMOS transistor $V_{th} = 0.5V$. Both the
transistors are matched exactly such that $\beta_n = \beta_p$. Find the unity gain
points (the values of input voltages V_{IL} , V_{IH} and corresponding output
 V_{out}) of the inverter characteristics assuming that the inverter is not
loaded.
- (b) Explain the latch up in CMOS. What are the remedies to avoid the 10
latch up ?
3. (a) Design a circuit for the function $\overline{A+(B+C)(D+E)}$ using CMOS logic. 10
Size all the transistors so that rise and fall time of the output of function
is equivalent to standard CMOS inverter with PMOS width is $2W$ and
NMOS width is W .
- (b) What do you mean by threshold voltage of MOSFET ? How do we 10
control ? Explain with the help of relevant mathematical equations.
4. (a) Explain the concept of pass transistor logic useful to implement logic 10
function. Explain limitations of PMOS/NMOS transistors and how it
can be taken care of.
- (b) Explain the method to design 4:1 MUX using pass transistor logic. 10
Draw the circuit diagram using NMOS pass transistors.
Also draw the stick diagram.

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5. (a) Explain constant field scaling. 10
Assuming a constant scaling factor of 0.7 for various critical MOSFET parameters, calculate the performance improvement in terms of package density, power dissipation, and speed for ideal CMOS process.
- (b) Draw the circuit diagram, stick diagram and layout using λ based design rules for the two inputs CMOS NAND gate. Use proper aspect ratio and color coding. 10
6. CMOS inverter is to be fabricated using n-well process. Discuss various steps involved in fabrication. Sketch the masking steps in cross sectional view giving mask sequence. 20
Mention the number of masks required in complete process.
7. Write short notes on any **four** :— 20
- (i) Custom and Semi custom design methods
 - (ii) Short channel effects in MOSFET
 - (iii) Design verification methods
 - (iv) VHDL in VLSI design
 - (v) Burried and Butting contacts
 - (vi) Comparison of ion implantation and diffusion.

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