02/12/08.

Con. 5417-08.

(a)

(b)

and addvisability for data transfers.

## (REVISED COURSE)

BB-8333

(3 Hours)

[Total Marks: 100

N.B.	(2)	Question No. 1 is compulsory.  Attempt any four questions out of the remaining questions.  State any additional data assumed, if necessary to answer.	
1.	(a) (b)	Explain the conditions under which the Pentium performs 'burst cycles' and only with timing diagram, explain the burst cycle from main memory to processor. Explain with a neat diagram, Pentium state transitions.	12
2.	(a) (b)	Explain the "Write Once" policy as implemented in the Pentium Processor with examples, assuming that Lz Cache is present.  Explain the functional Redundancy Check feature of the Pentium.	10
3.	(a) (b)	Explain the need and working of the Branch Prediction Logic. Explain clearly the structure of the BTB.  Explain the interrupt subsystem of the Pentium in detail.	10
4.	(a)	Explain the process of data transfer over the PCI Bus with following reference:  (i) Bus mastering and its latency  (ii) Data Phases  (iii) Priorities for bus masters.	15
	(b)	Write a detailed note on special cycle of the Pentium processor.	5
5.	(a)	Explain the function of the following PCI Bus signals –  (i) DEVSEL  (ii) FRAME  (iii) SDONE  (iv) PAR  (v) SBO	10
	(b)	What is meant by Bus Access Latency with reference to the PCI Bus. Also explain the function of the Latency timer.	10
6.	(a) (b)	Explain the basic features of a real time operating system (eg. QNX).  Explain the importance of "interrupt handler" in the QNX operating system.	12

Compare the USB and Rs-232C interspace and justify the choice in terms of speed 12

Explain the process of USB device enumeration of any USB device of your choice.