Con. 5458-08. **(REVISED COURSE)** **BB-8339**

(3 Hours) **[Total Marks : 100**

N.B. (1) Question No. **1** is **compulsory**.
(2) Attempt any **four** out of remaining **six** questions.
(3) Assume any **suitable** data wherever **required** but justify the same.

1. (a) Derive expression for current in saturation region from that of the linear region current equation. **20**
(b) Define Device Trans-conductance. What is its significance ?
(c) Explain why nFET pass transistor is said to pass only a week **logic '1'** and a strong **logic '0'** ?
(d) Explain the factors on which dynamic power dissipation depends.
(e) Compare between the semiconductor materials (Silicon and Germanium) for VLSI Technology.

2. (a) For a pMOS device if **10**
$\mu_p = 220\ cm^2/V\text{-}sec$ $\quad t_{0x} = 9{\cdot}5\ nm$
$\varepsilon_{0x} = 3{\cdot}9 \times 8{\cdot}85 \times 10^{-14}\ F/cm$ $\quad W = 12\ \mu m$ $\quad L = 0{\cdot}35\ \mu m$
$V_G = -5$ Volts $\quad V_{TH_p} = -1{\cdot}5$ Volts
Find Drain current if $V_{DS} = -2$ Volts.
(b) Find the expression for Threshold voltage of nMOS device also explain the effect of substrate potential (Body Effect) on Threshold and also discuss the effect on overall performance of the device. **10**

3. (a) Compare various loads used in Inverter circuit. Draw proper diagram and compare different parameters which characterize each type of Inverters. **10**
For a CMOS Inverter.
(b) $K'_n = \varepsilon_{0x}\ \mu_n = 140\ \mu A/V^2$ $\quad V_{TH_n} = 0{\cdot}7$ Volts **10**
$K_p = \varepsilon_{0x}\ \mu_p = 60\ \mu A/V^2$ $\quad V_{TH_p} = -0.7$ Volts
With $V_{DD} = 3{\cdot}0$ Volts
For obtaining symmetrical characteristics comment on the aspect ratios of load and the driver. Also determine the midpoint voltage.

4. (a) $F = \overline{a.b.c. + d}$ **10**
Consider the logical function as given above
(i) Design the CMOS logic gate that provides the function.
(ii) Is it possible to find an Euler graph for the circuit ? If so, construct the graph and also it to perform stick level layout. If not find a layout strategy for the GATE.
(b) State different methods of oxidation stating which method is suitable for different oxide layers in VLSI Technology. Compare oxide layer grown for short time and long time oxidation, for following specifications :— **10**
$A = 0{\cdot}05\ \mu_m/sec$ $\quad B = 0{\cdot}72\ \mu_m/s^2$
Short time $t = 0{\cdot}01$ hours $\quad$ long time $= 100$ hours.

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5. (a) An nMOS device is to be fabricated, describe its fabrication steps giving the mask sequence. Sketch the masking steps in cross-section view. **10**

   (b) Find resistance Rn for nMOS if electron mobility $\mu_n = 560\ cm^2/V\text{-}sec$, $t_{0x} = 10\ nm$, $\varepsilon_{0x} = 3{\cdot}9 \times 8{\cdot}85 \times 10^{-14}$ F/cm, and $V_G = 3{\cdot}3$ Volts $V_{TH_p} = 0{\cdot}7$ Volts **10**

   (i) if $W = 10\ \mu_m$ $L = 0{\cdot}5\ \mu_m$

   (ii) if channel width is increased to a value of $W = 22\ \mu_m$ while the channel length remains same.

6. (a) Explain the method to design 4 : 1 MUX using nMOS and CMOS (transmission gate) also draw stick diagram for both implementation. **10**

   (b) What is significance of testability in case of VLSI ? Explain the fault modeling with proper examples. Explain **Sa '0'** and **Sa '1'** fault modeling. **10**

7. Write a short notes on (any **four**) :— **20**

   (a) Design Rules and its significance

   (b) Burried and Butted contact in nMOS Technology

   (c) Scaling : its requirement and limitations

   (d) Super-buffers

   (e) Latchup problem in CMOS

   (f) Photolithography.