S.E. Sem 4 Etrx. Digital Design - II 02/12/08

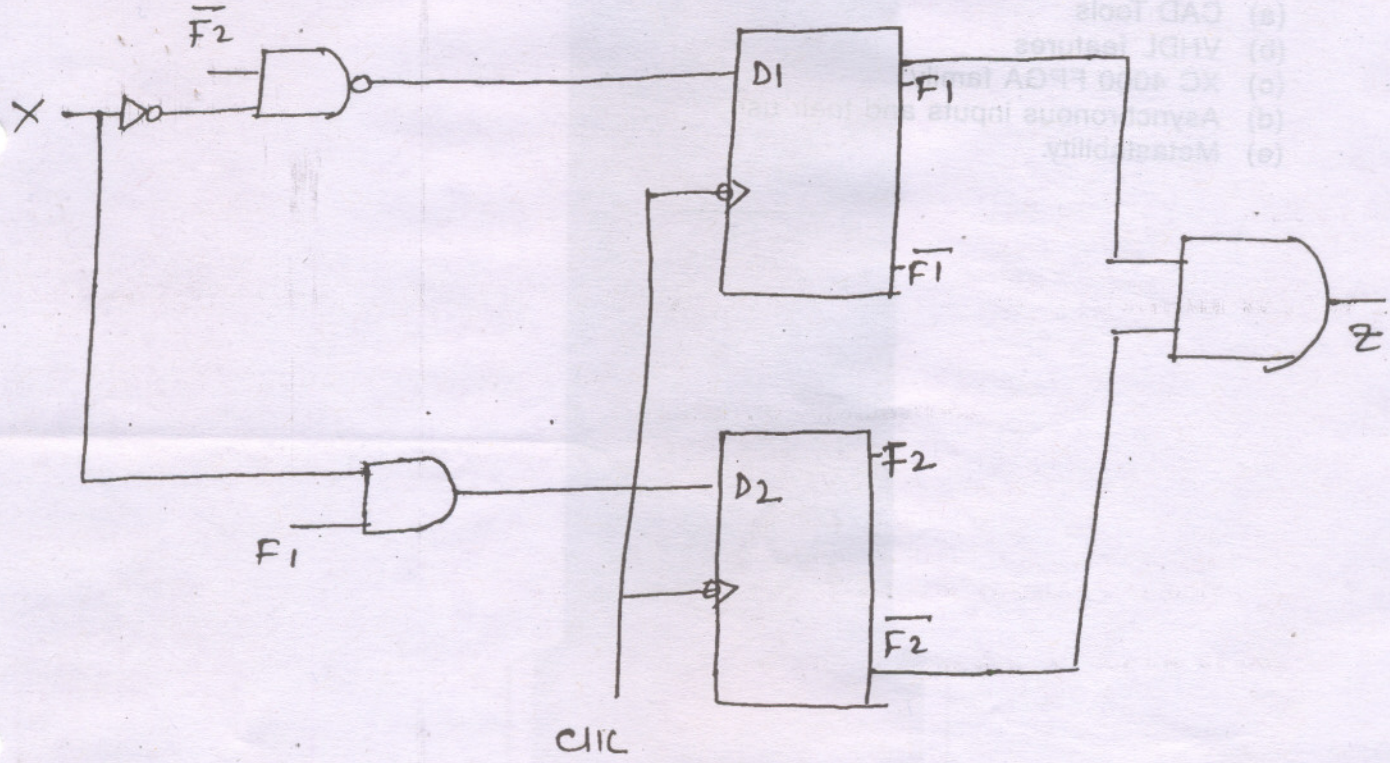
Con. 5027-08. RC-6092

(3 Hours) [Total Marks : 100

N.B. (1) Question No. **1** is **compulsory.**
(2) Attempt any **four** questions out of remaining **six** questions.
(3) **Figures** to the **right** indicate **full** marks.

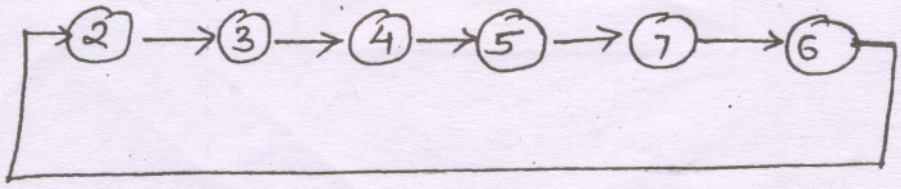
1. (a) Compare synchronous counters and asynchronous counters. 6
(b) Draw a switch debouncer using NAND gates and explain it. 6
(c) Design sequential m/c serial binary adder using JK F/F and NAND gates only. 8

2. (a) Analyze the sequential machine shown and obtain the state diagram for the same. 10



(b) Write a VHDL code for a left to right shift register with an enable input. 10

3. (a) Design a coin operated vending m/c that dispenses candy under following condition :— 10
(i) The machine accept nickels (= 5 cents) and dimes (= 10 cent)
(ii) It takes 15 cents for a piece of candy to be released from the machine.
(iii) If the 20 cents is deposited, the machine will credit the buyer with 5 cents and wait for the buyer to make second purchase.
Follow all the steps including state decomposition and state assignment rules in designing of above machine.
(b) Design a synchronous counters with JK F/F which runs through a sequence of 10



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4. (a) What are different types of shift registers ? Design 4 bit Johnson counter using 74194 universal shift register. **10**
   (b) Discuss various modes of operating IC 7490. Also include sequence table for various modes. **10**

5. (a) Explain SRAM architecture block diagram with timing diagram for read and write operation. **10**
   (b) Design a state machine that detects three or more consecutive 1's in a string of bits coming through an input line synthesis the circuit using D flip-flops. **10**

6. (a) Give the main features of Xilinx XC 9500 CPLD family. **10**
   (b) Discuss the main issues related to the estimation of Digital System Reliability. **10**

7. Write notes on (any **three**) :— **20**
   (a) CAD Tools
   (b) VHDL features
   (c) XC 4000 FPGA family
   (d) Asynchronous inputs and their use
   (e) Metastability.
