T.E. sem 5 (Rev.) EXTC.. Elements of Microelectronics. 20/12/08

ws Oct 08 323

Con. 6006–08. (REVISED COURSE) RC–6522

(3 Hours) [Total Marks : 100

N.B. : (1) Question No. **1** is **compulsory**.
(2) Attempt any **four** questions out of remaining **six** questions.

1. (a) Explain MOSFET capacitances. 10
   (b) Explain ion–implantation technique. 5
   (c) Define LS1, MS1 and VLS1 circuits. 5

2. (a) Explain with neat diagram the Czochralski (CZ) process. 10
   (b) Explain different short–channel effects in MOS transistor. 10

3. (a) Explain different types of scaling. 10
   (b) Explain with neat diagrams CMOS transistor fabrication process using Twin Tub process. 10

4. (a) Write a short note on λ based design rules for NMOS and CMOS. 10
   (b) Draw stic diagram and mask layout using λ based design rules of the CMOS NAND gate. 10

5. (a) Design CMOS logic gate for the following functions : 10
      (i) $F = \overline{ab + ac + bd}$
      (ii) $F = \overline{abc + ad}$.
   (b) Explain with neat layout of Butting and Buried contacts. 10

6. (a) What is Epitaxy ? What are the different epitaxial processes ? Explain one of them in detail. 10
   (b) Explain the following :– 10
      (i) Lateral PNP and Vertical PNP transistor.
      (ii) Rise time of EMD pull up inverter.

7. Write short notes on any **two** :– 20
   (a) Photolithography
   (b) MOSFET operation
   (c) Different IC Resistors.