

(Lib)

Q.B. (1) Question No.1 is compulsory.

(2) Solve any four from remaining six questions.

(3) Assume the suitable data if necessary.

1. (a) Design the W/L ratio of the NMOS transistor used in resistive load inverter with $V_{TO} = 1V$, $V_{DD} = 5V$ and the permissible power dissipation is 0.5 mw , $k'_n = 25 \mu\text{A}/\text{V}^2$. Assume $V_{OL} = V_{DS} = 0.25V$. 5
- (b) Arsenic is diffused in silicon with a doping concentration of $5 \times 10^{15} \text{ atoms/cm}^3$. Arsenic doping assumes a Gaussian profile. Arsenic is diffused for 30 minutes and a junction depth of $20 \mu\text{m}$ is achieved with a surface concentration of $2 \times 10^{18}/\text{cm}^3$. Find the diffusivity of Arsenic. 5
- (c) A chip based on CMOS circuit with a supply of $3V$ suppose to work at 10MHz . The chip has 20 devices in it. The total transfer of charge per device is 40nc . Calculate the average power dissipation and also calculate the worst case power dissipation when all the devices switch simultaneously. 5
- (d) Compare NMOS NAND with NMOS NOR with respect to their (W/L) requirements of driver transistors needed to have symmetric inverter with inverter ratio equal to 1. 5
2. (a) A device is fabricated with Al gate with work function potential of 0.754 volt . The substrate doping of NMOS is $3 \times 10^{16}/\text{cm}^3$. Determine the thickness of oxide assuming the $Q_{OX} = 1.6 \times 10^{-8} \text{ c/cm}^2$. The inversion occurred at $V_G = 0.65 \text{ V}$. [$n_i = 1.45 \times 10^{10} /\text{cm}^3$, $\epsilon_{OX} = 0.345 \times 10^{-12} \text{ F/cm}^2$, $E_{si} = 1.035 \times 10^{-12} \text{ F/cm}^2$] 10
- (b) Explain ION implantation and compare it with diffusion clearly stating the advantages and disadvantages. 10
3. (a) What is band bending ? Explain in brief. What is flatband condition and how will you achieve this ? 3 + 4 + 3 = 10
- (b) Design a CMOS NAND gate (two I/p) which is equivalent to the CMOS inverter with $K_R = 2$. 10
4. (a) Explain the method to design 4:1 MUX using pass transistor logic. Draw the circuit diagram using NMOS pass transistors. Also draw the stick diagram. 10
- (b) Draw the layout using λ rules for two input NAND gate using NMOS enhancement – depletion technology with $\left(\frac{W}{L}\right)_L = \frac{1}{4}$ and $\left(\frac{W}{L}\right)_D = \frac{1}{2}$. 10
- Take minimum diffusion width = 3λ for any transistor.
5. (a) Compare constant voltage and constant field scaling on the basis of parameters listed :— 10
- (i) Power density (ii) Driving capacity and
- (ii) Time delay (iv) Power delay product.
- (b) State the conditions required for the symmetric CMOS inverter. Prove that $K_R = 1$ with the help of derivation for K_R and conditions for symmetry. 10

6. (a) Explain the concept of pass transistor. What are limitations of PMOS and NMOS pass transistor ? Explain it and also suggest remedy to overcome the limitations. 2 + 6 + 2 = 10
- (b) Explain the short channel effects with respect to the following points :—
- (i) Subthreshold condition 2
 - (ii) Channel length modulation effect 3
 - (iii) Velocity Saturation and Mobility degradation 3
 - (iv) Drain induced barrier lowering. 2
7. Write short notes on any **three** of the following :— 20
- (a) Butting and Buried Contacts in VLSI
 - (b) CMOS latchup and prevention
 - (c) Custom and semicustom design methods
 - (d) Photolithography in IC fabrication.
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