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M.E | ETRX | sem I

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126 : 2nd-AExm 09-Mina

micro and sys. - I

10 30 to 12:30

Con. 5344-09.

B|3-6110

Microprocessor & Systems - I

(3 Hours) [Total Marks :100

N.B.: (1) Question No. **1** is **compulsory.**
(2) Attempt any **four** questions out of remaining questions.

1. Design SBC with following specifications :— **20**
   (a) 80386 DX operates at 25 MHz
   (b) Firmware support of 256 KB using 32 KB EPROM devices
   (c) Data memory support of 1 GB using 512 MB SRAM devices
   (d) 2 input and 2 output ports all interrupt driven and all 32-bits wide.
   Draw a neat diagram. Show memory and I/o maps and decoding logic used.

2. Draw the follcwing diagrams and explain :— **20**
   (a) Segment translation mechanism.
   (b) Page translation mechanism, compare and contrast Segmentation and Paging.

3. (a) Explain IRQZ redirect mechanism in ISA bus. **10**
   (b) Explain ISA DMA subsystem. **10**

4. (a) Explain how shareable interrupts are serviced in ISA. **10**
   (b) Explain ISA timer. **10**

5. Explain what is TSS ? Draw the diagram for Indirect task switching. Explain each step in detail. **20**

6. (a) Explain various Write policies used with cache memory. **10**
   (b) Explain how 82385 DX determines cache hit and cache miss. **10**

7. Explain the architecture of 80386 EX with a diagram. Explain the function of configuration registers. **20**