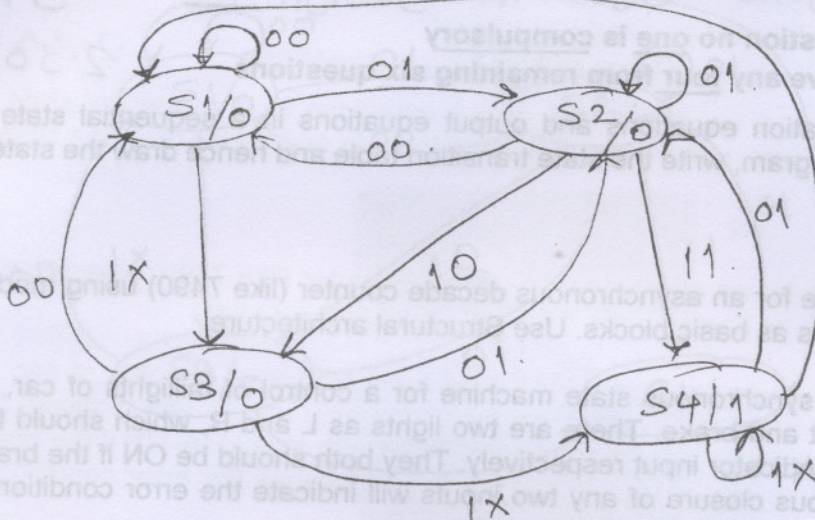


5a) Write a VHDL code for the state Diagram shown. Make use of "Process" statement.



b) What will be the output on q with respect to clk and d if the following VHDL code is simulated? Explain with help of waveform. 08

```

architecture Behavioral of test_prog is
begin
    Process(clk)
    begin
        if (clk'event and clk = '1') then
            if(reset = '1') then
                q<= '0';
            else
                q<= d;
            end if;
        end if;
    End process;
end Behavioral;
    
```

ps	ms	X=0	X=1
A	B	0	C
B	B	0	D
C	B	0	C
D	E	0	C
E	B	0	C

6a) Draw and explain logic diagram of 64 X 1 diode ROM Use two-dimensional decoding. 10

b) With reference to XC 9500 CPLD family answer the following questions 10

Explain architecture of functional block
Which are the analog controls available in I/O block of XC9500

7a) Design a Moore Sequential machine that detects serial input sequence of X = "010110". Output Z goes high when such a sequence is detected. Use JK flip-flops and logic gates for the design. 10

b) Design a synchronous counter that counts the following sequence using D flip-flops. 10

