

Con. 5373-09.

T. E. (ETRX) Sem VI

SP-8024

Computer Organisation (3 Hours)

[Total Marks : 100

15/12/09

1. B. : (1) Question No. 1 is **compulsory**.
 (2) Attempt any **four** out of remaining **six** questions.
 (3) Assume **suitable** data wherever **necessary** and justify the **same**.
 2-30 to 5-30

- Q.1 a. Show Direct mapping for the following memory structure 10
 Main Memory=64KB
 Cache Memory=128 blocks of 16 words each
- b. Solve using Booth's Algorithm 05
 (-7) x (3)
- c. IEEE 754 format for floating point no. representation. 05
- Q.2 a What is microprogramming? Draw and explain microprogrammed Control unit. 10
- b. What is bus contention? How is it resolved by using bus arbitration? 10
- Q.3 a Explain the concept of Cache memory, with reference to principle of Locality of reference, hit ratio and different Cache architectures. 10
- b. If access time of cache memory (t_{A1})= 10^{-7} sec 10
 If access time of main memory (t_{A2})= 10^{-2} sec
 Efficiency (E)=0.9, find Hit ratio(H)
- Q.4 a. What is virtual memory? Explain how paging is useful in Implementing Virtual memory. 10
- b. Explain data hazards in a linear pipelining system and prove that for a K stage pipelining the speed up factor=K 10
- Q.5 a What is Cache coherency? why is it needed? Explain techniques to achieve it. 10
- b. Which are different I/O accessing techniques? 10
- Q.6 a. Explain various steps taken by CPU in interrupt processing. 10
 Explain how multiple devices share a single interrupt line.
- b. State and explain various DMA transfer modes 10
- Q.7 a Explain various addressing modes of Pentium 10
- b. Explain various characteristics of memory 10