17/12/2011

WT-Sept.-11- 171

B.E (E&TX) Sem VII (R)

Communication Network

Laboratory

Con. 6625–11. **(REVISED COURSE)** **MP–5578**

(3 Hours) **[Total Marks : 100**

N.B. : (1) Question No. **1** is **compulsory**.
(2) **Figures** to the **right** indicate **full** marks..
(3) Assume **suitable** data wherever **necessary**.

1. (a) Explain the property of data transperency with reference to HDLC ? **5**
   (b) Differentiate btween In Band Signalling and Out Band Signalling. **5**
   (c) What are conditions to be satisfied for a valid CRC generator polynomial. Draw block diagram of CRC generator. **5**
   (d) Explain how Fast Ethernet differs from 10 base T. **5**

2. (a) Derive the transmission efficiency of Go back N ARQ. State effect of bit error rate and delay bandwidth product on transmission efficiency. **10**
   (b) Explain spanning tree algorithm with respect to frame forwarding, address learning and loop resolution. **10**

3. (a) Identify the address class of following IP addresses :– **10**
   200·58·20·165;128·167·23·20. Also perform CIDR aggregation of following :–
   |22 IP addresses : 128·56·24·0|22; 200·96·87·0|22.
   (b) What is essential difference between Dikstra algorithm and Bellman Ford algorithm ? Explain these algorithms in brief. **10**

4. (a) Error control procedures are specified in each layers of OSI reference model. Indicate the layers at which each of following errors might occur :– **10**
      (i) Noise on transmission link converts 0 bit 1 bit.
      (ii) A packet is routed to wrong destination.
      (iii) A packet switching network delivers a data unit to a terminal attached to it out of sequence.
      (iv) A printer printing halfway through a line is suddenly commanded by mistake to return to the begining of line.
      (v) During half duplex mode session the transmitting user starts recieving data from the user at other end.
   (b) Sketch non blocking switches with N = 32 and group size n = 4 for a 3 stage space division switch and a TST switch. Which is better option ? Why ? **10**

5. (a) List categories of UTP cables. How is noise interference minimised in twisted pair ? **5**
   (b) What is delay distartion with respect to a transmission medium ? How it can be corrected ? **5**
   (c) Explain ADSL with respect to channel configuration and modulation technique. **10**

6. (a) Distinguish between implicit congestion signalling and explicit congestions signalling. Discuss three general approaches for explicit congestion signalling. **10**
   (b) Distinguish between following token reinsertion strategies :– **10**
      (i) Single token operation
      (ii) Multiple token operation
      (iii) Single frame operation.

7. Write short note on :– **20**
   (a) SONET
   (b) Berkcley API
   (c) ARQ Techniques

7. Write short note on :– 20

(a) SONET
(b) Berkcley API
(c) ARQ Techniques
(d) ISDN.

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13/12/2011 BE ETRX VII CBSGS
VLSI Design

Con. 6505-11. (REVISED COURSE) MP–5590

(3 Hours) [Total Marks : 100

N.B. : (1) Question No.1 is **compulsory**.
(2) Attempt any **four** out of remaining **six** questions.
(3) Assume **suitable** data, wherever **required**.

1. Answer any **FOUR.** **(20)**

(a) Consider a MOS structure with a p-type semiconductor substrate doped to Na = $10^{16}/cm^3$, a SiO_2 insulator with a thickness of 500 A° and an oxide charge density of $10^{11}/cm^2$, and a polysilicon gate. Calculate the Flat band voltage. Assume that $\phi_{GC} = -1.1$ V.

(b) What is Subthreshold conduction? What are the factors controlling the subthreshold current in long channel and short channel MOSFET?

(c) What is Velocity Saturation? How does it effect the I-V Characteristics of a short channel MOSFET?

(d) Depletion mode n-channel device are not complementary to enhancement mode n-channel transistor and can not match up with a p-channel enhancement mode transistor as load in an inverter circuit. Explain.

(e) "The boundaries of the valid input signal regions that define the Noise Margins in an inverter (V_{IH} & V_{IL}) are defined as the voltage points where the magnitude of the inverter voltage gain is equal to unity". Explain why?

2. (a) Explain the complete fabrication process steps for a CMOS inverter using n-well process with the help of cross sectional diagrams for all important masking steps. **(10)**

(b) Consider a silicon-gate PMOS transistor with the following parameters: **(10)**
Substrate doping $N_D = 10^{16}/cm^3$, Gate doping $N_D = 10^{20}/cm^3$, $Q_{OX} = 4 \times 10^{10}$ qC/cm^2,
$t_{OX} = 0.10$ μm

(i) Determine the threshold voltage V_{TO} under zero bias at room temperature. Note that $\epsilon_{OX} = 3.97\epsilon_0$ and $\epsilon_{si} = 11.7\epsilon_0$.

(ii) Determine the type (p-type or n-type) and amount of the channel implant (N_I/cm^2) required to change the threshold voltage from V_{TO} to - 1 V and + 3 V.

3. (a) In the inverter circuit what is meant by $Z_{p.u}$ and $Z_{p.d}$? Derive the required relation between $Z_{p.u}$ and $Z_{p.d}$ if an NMOS inverter is to be driven from another NMOS inverter. **(10)**

(b) An enhancement mode n-channel MOSFET has the following parameters. **(10)**
Threshold voltage $V_T = 0.8$ V, Channel length modulation coefficient $\lambda = 0.05/V$,
$\mu_n C_{ox} = 20\ \mu A/V^2$, $\left(\frac{W}{L}\right) = 20$
Find the drain current for the following cases:

(i) $V_g = 5$ V, $V_D = 4$ V, $V_S = 2$ V

(ii) $V_g = 2.8$ V, $V_D = 5$ V, $V_S = 1$ V

[TURN OVER

4. (a) A reference inverter has $\left(\frac{W}{L}\right)_n = \frac{1}{1}$ and $\left(\frac{W}{L}\right)_p = \frac{3}{1}$. Draw the schematic and the stick diagram of a two input NAND gate and calculate the $\left(\frac{W}{L}\right)$ ratios of transistors based on reference inverter design. (10)

(b) Draw the mask layout for the circuit designed in Question 4(a) in n-substrate and p-well. (10)

5. (a) Compare constant field scaling with constant voltage scaling and state advantages and limitations in both the methods. Show analytically how delay time, power density and current density are affected in terms of scaling factors in both the type of scaling methods. (10)

(b) Implement the following Boolean function in CMOS logic: (10)

$Y = \overline{(D+E+A).(B+C)}$

Draw the optimised stick diagram of the logic gate using Euler path.

6. (a) Draw the p-well CMOS inverter and explain the latch up effect in it. Why latch up must be prevented and what are the remedies to avoid the latch up problem in the circuit? (10)

(b) Implement a 2:1 multiplexer circuit using CMOS transmission gates. Write a Verilog module for the circuit at switch level of abstraction. Write a test bench to check the functionality of the circuit. (10)

7. Write short notes on any **three**: (20)
   (a) Ion implantation
   (b) MOS capacitance
   (c) Design rules and their necessity
   (d) Short channel effects.

8/12/2011 BE ETRX VII CBSGS Power Electronic & Drives

211 : 2ndHf11C.mk

Conf. 6298-11. **(REVISED COURSE)** **MP-5572**

(3 Hours) **[Total Marks : 100**

N.B. (1) Question No. **1** is **compulsory**.
(2) Attempt any **four** questions out of the remaining **six** questions.
(3) **Figures** to the **right** indicate **full** marks.
(4) Assume **suitable** additional data if **necessary.**

1. (a) Explain how semiconverter provides better power factor compared to full converter when both are working as rectifiers with R-L load. **5**
   (b) Explain why separately excited d.c. motor is used in most of the applications where variable speed is required compared to ordinary shunt d.c. motor. **5**
   (c) Draw torque-speed characteristics for the following control circuits for squirrel cage a.c. induction motor. **5**
      (i) Variable stator voltage control
      (ii) V/f control.
   Why the second control circuit is used in most of the industrial applications ?
   (d) Give advantages of flyback converter compared to forward converter. **5**

2. (a) Explain how full converter can be operated as — (i) rectifier (ii) inverter using appropriate waveforms. What are conditions for successful inverter operation ? **10**
   (b) Draw circuit diagram of dual converter and explain its working. Give relation between firing delay angles of two converters when the circuit is operating in circulating current mode. Give advantage of this mode of operation in d.c. motor control. **10**

3. (a) Explain working of any voltage commutated chopper circuit using SCR's. Draw relevant voltage/current waveforms. **10**
   (b) A d.c. separately excited motor is driven by class A chopper circuit fed from 220 V d.c. supply. If motor rating is 110 V, 75 A, 750 RPM with R_a = 0·1 Ohm and motor speed required is 500 RPM at half the full load torque determine duty cycle of chopper. **10**
   If on time of chopper is 1 millisecond determine frequency of the chopper circuit. Assume that field winding is fed from fixed 110 V d.c. supply.

4. (a) Explain working of McMurray bridge inverter using circuit diagram and appropriate waveforms. **10**
   (b) Explain working of multiple pulse PWM with sinewave reference signal. Discuss the application of the circuit in a.c. motor control. **10**

5. (a) Explain constant torque and constant power operation of separately excited d.c. motor. Give schematic diagram of control circuit. **10**
   (b) A separately excited d.c. motor is driven by full converter bridge operating on 250 V single phase 50 Hz supply. The motor ratings are 110 V, 950 RPM, 25 Amps with R_a = 0·1 Ohm. Find the firing delay angle α in the following two cases :— **10**
      (i) Motoring mode, 700 RPM, half the full load torque
      (ii) Braking mode, 650 RPM, half the full load torque.

6. (a) Explain using schematic diagram how slip power recovery technique can be used to control a.c. motor speed above and below synchronous speed. What is the advantage of this technique ? 10

(b) Using block diagrams discuss different configurations of UPS. 10

7. Write short notes on any **two** of the following :— 20

(a) Converter types used in SMPS

(b) Selection of battery in UPS

(c) Effect of source inductance in converter.

22/12/2011 BE ETRX Sem-VII (Rev)
Digital Image Processing

PR-Oct. (1) 178
Con.6842-11.

MP-5593 Design

(REVISED COURSE)

(3 Hours) [Total Marks : 100

N.B. : (1) Question No. 1 is **compulsory.**
(2) Attempt any **four** questions out of remaining **six** questions.
(3) **Assume any suitable** data if **necessary.**

1. State whether the following statements are **true** or **false.** Justify your answer– 20
   (a) Low pass filter is smoothening filter.
   (b) Huffman coding is a lossless data compression technique.
   (c) Median filter is used to remove salt and pepper noise.
   (d) Quality of picture does not depend on the number of pixels and gray levels that represent the image.

2. (a) An image segment of 4 × 4 size with 3 bits per pixel is shown below. Perform the following operations– 10
   (i) Image Negative
   (ii) Bit plane slicing–

0	7	1	2
2	5	3	2
1	4	5	6
3	2	5	2

   (b) What do you understand by sampling and quantization with respect to digital image processing ? How will you convert an analog image into a digital image. 10

3. (a) Discuss advantages of homomorphic filtering. Also explain the steps of homomorphic filtering with the help of a neat block diagram. 10
   (b) Name different types of image segmentation techniques. Explain the splitting and merging technique with the help of an example. 10

4. (a) Compare between contract stretching and histogram equalization. 10
   (b) What do you understand by Hadamard Transform ? Write a 4 × 4 Hadamard Matrix. Discuss application of Hadamard Transform.

5. (a) Name and explain different types of redundancies in digital image. 10
   (b) Explain image compression model with the help of a neat block diagram. 10

6. (a) How will you detect following in a digital image ? 10

(i) Point

(ii) Line

(iii) Edge.

(b) Define two dimensional Discrete Fourier Transform (2D – DFT). Explain the properties of 2D – DFT in detail. 10

7. Write short notes on the following :– 20

(a) Biometric Authentication

(b) Dilation and Erosion

(c) Digital Watermarking

(d) Lossless Compression.

22/12/2011 BE (ETRX) VII (Rev)
Elective II Wireless Communication

271 : 2ndHf11C.mk

Con. 6847-11. **(REVISED COURSE)** **MP-5582**

(3 Hours) **[Total Marks : 100**

N.B. (1) Question No. **1** is **compulsory**.
(2) Solve any **four** questions out of remaining **six** questions.
(3) **Figures** to the **right** indicate **full** marks.

1. (a) Explain Umbrell Cell approach in Cellular System. **20**
(b) Explain soft hand off in CDMA.
(c) Explain CDMA 2000 MAC and LAC sub layer.
(d) Explain spectral efficiency and pulse shaping in OFDM.

2. (a) Explain cell sectoring and cell splitting in detail to improve coverage area and capacity. **10**
(b) A hexagonal cell within a four cell system has a radius of 1·387 km. A total of 60 channels are used within the entire system. If the load per user is 0·029 Erlangs and λ = 1 call/hour. Compute the following for an Erlang C system that has a 5% probability of a delayed call. **10**
(i) How many users per square kilometer will this system support.
(ii) What is the probability sheet a delayed call will have to wait for more than 10 seconds ?
(iii) What is the probability that a call will delayed for more than 10 seconds ?

3. (a) Explain GSM system architecture in detail with interfaces. **10**
(b) Explain OFDM block diagram and derive the mathematical expression for OFDM signal. **10**

4. (a) Explain variable data transmission and power control in detail with reverse CDMA. **10**
(b) Explain the need of spreading the sequence in CDMA. Explain Direct sequence spread spectrum with transmitter and receiver block diagram. **10**

5. (a) Explain in detail the working of RAKE receiver. **10**
(b) Explain in detail CDMA 2000 layered structure. **10**

6. (a) Explain in detail different traffic channels and control channels in GSM. **10**
(b) Draw and explain uplink and downlink CDMA (IS-95) models. **10**

7. Write short notes on :— **20**
(a) Pilot channel in CDMA
(b) Frame structure of GSM
(c) Bluetooth
(d) Zigbee network.

2/12/2011 BE ETRX Sem-VII (Rev)
Filter Design

101: 2nd Half-Exam.-11 mins (a).

Con. 6135-11.

(REVISED COURSE)

MP-5584

(3 Hours)

[Total Marks : 100

N. B. : (1) Question No. 1 is **compulsory**.
(2) Attempt any **four** questions out of the remaining **six** questions.
(3) **Figures** to **right** indicate **full** marks.
(4) Assume **suitable** data if **necessary**.

1. Attempt any **Five** of the following: 20

a) Compare Butterworth and Chebysev filters in terms of frequency response and order of the filter.
b) State the advantages of switched capacitor filter.
c) Compare between FIR and IIR digital filters.
d) Explain the working principle of basic Weiner filter.
e) Explain in brief any one application of Multirate DSP.
f) Write a short note on Quadrature mirror filter (QMF) bank.
g) Digitize the analog transfer function using impulse invariance method.

$$H_a(s) = \frac{2}{(s+1)(s+3)}$$

2. a) What is FDNR ? State its properties. Explain synthesis of lowpass functions using FDNRs. with Op-amps 10

b) Explain the effect of Decimation and Interpolation in time and frequency domains with examples. 10

3. a) Design lowpass FIR linear phase filter with 11 coefficients using Hamming window for the following specifications. 10

Passband Frequency : 0.25 KHz

Sampling Frequency : 1 KHz

b) Design a Butterworth filter using impulse invariance and Bilinear transformation . for the following specifications. Assume $T = 1sec.$ 10

$$0.8 \leq |H(e^{jw})| \leq 1 \quad for \quad 0 \leq |w| \leq 0.2\pi$$

$$|H(e^{jw})| \leq 0.2 \quad for \quad 0.6\pi \leq |w| \leq \pi$$

4. a) Explain the design steps of FIR filter using frequency sampling method.Give merits and demerits over window method. 10

b) Design a Chebyshev-I bandstop digital filter with the following specifications: 10

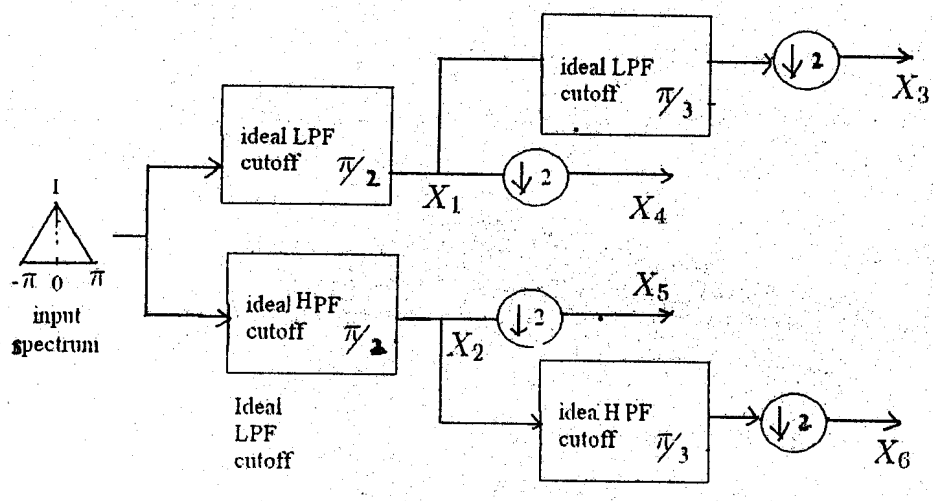
Passband range: 0 to 275 Hz and 2KHz to ∞
Stopband range: 550 Hz to 1000 Hz
Sampling Frequency : 8 KHz
Passband attenuation (α_p)= 1 dB.
Stopband attenuation (α_s)= 15 dB.
Use BLT and Assume T=1 sec.

[TURN OVER

5. a) Prove that $s = \frac{2}{T}\frac{1-z^{-1}}{1+z^{-1}}$ and $w = 2.tan^{-1}\frac{\Omega T}{2}$ in bilinear transformation. Also explain mapping between s-plane and z-plane. 10

   b) Describe Leapfrog realization technique in detail. 10

6. a) Draw the DTFT spectrums at points $X_1, X_2, X_3, X_4, X_5, X_6$ shown in Figure below. 10



   b) Explain the concept of subband coding. 05

   c) What are conditions that must be imposed on impulse response of FIR filter to obtain linear phase response? Idenify which of impulse of the following will give linear phase response? Why? assume 4^{th}sample as a origin. 05

$$h_1(n) = (1, 3, 4, 2, 4, 3, 1)$$

$$h_2(n) = (1, 3, 4, 2, 1, 3, 4)$$

7. Write short note on any four: 20

a) Kaiser Window
b) LMS algorithm
c) Frequency Warping effect in BLT
d) Applications of adaptive filters
e) Lowpass to Bandpass analog frequency transformation
f) Matched Z-transform.