12/12/11 BE ETRX VIII CRED
Advanced Networking Technologies

Con.6566-11. **(REVISED COURSE)** **MP-5179**

(3 Hours) **[Total Marks : 100**

N.B.: (1) Question No. **1** is **compulsory**.
(2) Solve any **four** from remaining **six** questions.
(3) **Figures** to the **right** indicate **full** marks.

1. (a) What are the functions of Network Layer ? **5**
   (b) With help of a suitable sketch explain Optical Networking in brief. **5**
   (c) Explain frame relay in brief. **5**
   (d) Discuss the need of Network Security. **5**

2. (a) Explain in detail Repeaters, Hubs, Routers and Gateways. **10**
   (b) Explain in detail ATM Adaptation Layer (AAL). **10**

3. (a) What do you mean by Network Layer Design ? Explain. **10**
   (b) Discuss the various fields in IPv4 frame. **10**

4. (a) Describe Network Security safeguard in detail. **10**
   (b) With respect to Network Management explain the following :— **10**
      (i) Documentation
      (ii) OAM & P.

5. (a) Describe the various wireless LAN technologies. **10**
   (b) Explain in brief ICMP. **5**
   (c) With the help of a neat sketch explain DWDM. **5**

6. (a) Explain ATM cell format in brief. **5**
   (b) Compare and contrast Ubiquitous and Hierarchical access. **10**
   (c) Explain in brief Layer 7 filtering. **5**

7. Write short notes on following :— **20**
   (a) Subnetting
   (b) Remote Monitoring
   (c) Congestion Control
   (d) VoFR.

16/12/2011 BE ETRX VIII (Rev) ES & RTP

Con. 6943-11. (REVISED COURSE) MP–5173

(3 Hours) [Total Marks : 100

N.B. : (1) Question No.**1** is **compulsory**.
(2) Answer any **four** of the remaining **six**.
(3) Draw **neat** diagram and assume suitable data wherever **required**.

Q.1 a) Explain Task and Task states. 5

b) Explain Embedded memories. 5

c) Differentiate between Object Oriented and Procedure language. 5

d) Explain SPI interface. 5

Q.2 a) Design a FSM (Finite State Machine) for a simple elevator control system. The building has three total floors (G+2). Each floor has a call button and there are three buttons inside the elevator to choose the desired floor. Discuss the operation of the system through the FSM. 10

b) What is bounded and unbounded priority inversion problem? Explain with a suitable example what is Priority Inheritance protocol? 10

Q.3 a) Discuss various types of Semaphore in detail. 10

b) Explain Waterfall model of embedded software development. 10

Q.4 a) Explain operating modes of ARM7 processors. 10

b) Briefly explain Exceptions of ARM7. 10

Q.5 a) Explain address space (Memory map) of MSP 430 10

b) Explain basic clock model of MSP 430. 10

[TURN OVER

Q.6 a) A real time program has three tasks with following characteristics:- 10

	Priority	Period	CPU time
T1	1	6	2
T2	2	18	14
T3	3	36	6

Determine whether the program will meet its deadline if scheduled according to priorities and with pre-emption.

b) Explain in detail Mutex, Pipes, Queue and Mailboxes. 10

20

Q.7 Write short note on any 4

a) Interprocess communication

b) Programming models

c) Digital signal controllers

d) Black box and White box testing

e) Difference between RS232 and RS 485.

7/12/14 BE/ETRx/(Rev)-VIII

Robotics & Automation

AGJ 2nd half (y) 30

Con. 6277-11. (REVISED COURSE) MP–5185

(3 Hours) [Total Marks : 100

N.B. : (1) Question No. **1** is **compulsory**.
(2) Attempt any **four** out of remaining **six**.
(3) **Figures** to **right** indicate **full** marks. **'all'** questions carry **equal** marks.
(4) Assume **suitable** data wherever **necessary**.

1. Answer the following questions:

A. Why inverse kinematics problem is not unique and direct kinematics problem is unique? **05**

B. Why is the SCARA arm more ideal for assembly applications? **05**

C. Write short note on classification of robots **05**

D. List Programming Languages used for PLC, Explain any One Language in brief. **05**

2. A. Differentiate between direct kinematics and inverse kinematics problems. **10**

B. Obtain the Inverse Kinematics solution of the 4 axis Adept - 1 SCARA robot with its IK algorithm starting from the arm matrix. Explain Each joint variable computation in brief. **10**

3. A. What are the considerations for applying DH algorithm? Explain the Direct kinematics solutions for a three axis planar robot. **10**

B. Define total work envelope, joint space work envelope, dexterous work envelope with their relevant formulas and Illustrate these for any one robot arm with a neat sketch. **10**

4. A. Derive the Three fundamental rotation matrices R1 (θ), R2 (θ) and R3 (θ) with the help of neat sketches. **10**

B. What is trajectory planning? Explain in brief how continuous motion path trajectory is planned. **10**

5. A. What is robot task planner? Explain in brief with the help of a block diagram **10**

B. Explain structure of Relay Sequencers in brief. **05**

C. What are advantages of PLC; List examples of PLCs and their manufactures. **05**

6. A. Compare the relative merits and demerits of different structured illumination techniques **10**

B. Explain structure of Timer and Counter functions; Hence give one example of each. **10**

7. Write short notes on **(Any TWO)** : **20**

A. Robot Specifications

B. Shape analysis of objects

C. Gross & Fine Motion planning

100: 2nd Half-Exam.-11 mina (a).

1/12/2011

B.E. (ETRX) VIII

Con. 6144-11. (REVISED COURSE) Advance. VLSI Design. MP-5170

(3 Hours) [Total Marks : 100

N. B. : (1) Question No. 1 is **compulsory**.
(2) Answer any **four** out of remaining **six** questions.
(3) Assume any **suitable** data wherever required and justify the **same**.

1. A. An nFET with L=0.5μm is built in a process where $K_n'=100\mu A/V^2$ and $V_{tn}=0.7V$. The gate to source voltage is set to a value of $V_{GSn}=V_{DD}=3.3V$. Calculate the required channel width to obtain a resistance of $R_n=950\Omega$ (use value of η= 1). 5
   B. Draw analog design octagon and explain its significance. 5
   C. Explain pipelined design concept. 5
   D. Explain low power design considerations. 5

2. A. What is the cell ratio and pull up ratio of 6T SRAM cell. How does these affect the read/write operation. 10
   B. Explain cross coupled differential sense amplifier with circuit diagram which is used in SRAM cell. State the advantages over other differential sense amplifiers. 10

3. A. What are the parasitic elements of interconnect wire and how it affects electrical behavior of the circuit. 10
   B. Explain modeling of RC delay of interconnect wire using distributed RC model. How this delay can be reduced? 10

4. A. What are the requirements of a clock signal and list the points to be considered in clock distribution. 10
   B. What are the different clocking strategies employed in VLSI systems. Discuss 'H tree' clock distribution in high density CMOS circuits. 10

5. A. Implement 4 bit adder using Carry Look Ahead (CLA) principle. 10
   B. Stat the need of input and output circuit. Explain with neat diagram the schematic and design considerations for the same. 10

6. A. Explain EEPROM using floating gate NMOSFET 10
   B. What is cross talk in integrated circuits? Explain various methods to reduce it. 10

7. A. Implement the following function using NOR-NOR implementation for a PLA
      i) Y1 = ab + a'c
      ii) Y2 = a'bc + abc
      iii) Y3 = a'b + ac 10
   B. Explain the need of frequency compensation in operational amplifiers. 10