BE | ETRX | VII (OLD) 26/11/12

F. T & A.

Con. 9445–12. **(OLD COURSE)** **KR-2310**

(3 Hours) **[Total Marks : 100**

N.B. : (1) Question No. **1** is **compulsory**.
(2) Attempt any **four** of the remaining **six** questions.
(3) Assume **suitable** data wherever required and justify the **same**.

1. Answer the following questions (any **five**) :– **20**
   (a) Show that the zero locations of FIR filter occur at reciprocal locations.
   (b) Compare and contrast FIR and IIR filters.
   (c) What is the need for linear phase response in FIR filters ? State the condition for FIR filter, to display linear phase characteristics.
   (d) How are gain and alternation related on linear and decibel scale ? Illustrate the magnitude and phase characteristics of four classical filters.
   (e) Justify the statement 'Ideal filter characteristics are not realisable.'
   (f) Explain the characteristics of different window functions.

2. (a) Design a lowpass filter (FIR) with cut-off frequency of 5 KHz and sampling frequency of 20 KHz using flamming window function. Assume N = 9. **10**
   (b) Explain the impulse invariance (IIR) method of filter design in digital domain. **10**

3. (a) Prove that $S = \frac{2}{T}\left[\frac{1-z^{-1}}{1+z^{-1}}\right]$ and $W = 2\tan^{-1}\left[\frac{\Omega T}{2}\right]$ in bilinear transformation. Explain the mapping between the S-domain and Z-domain. **15**
   (b) Check for linearity the following filter functions. **5**
   $y(n) = x(n) - 7x^2(n-1)$
   $y(n) = 3x(n-1) + 3x(n+2)$

4. (a) Discuss the design steps for realisation of digital lowpass filter having Butterworth characteristics. **10**
   (b) Derive the expression for filter under N, M digital Butterworth filter realisation. **10**

5. (a) Determine the coefficient of linear phase FIR filter of length N = 15 and having frequency response as below. **10**

$$H\left(\frac{2\pi k}{15}\right) = \begin{cases} 1 & k = 0, 1, 2, 3 \\ 0.4 & k = 4 \\ 0 & k = 5, 6, 7 \end{cases}$$

   (b) Compare and contrast impulse invariance and bilinear transformation technique of digital filter design (IIR). **10**

6. (a) Explain in brief the design steps for FIR filter design using the frequency sampling technique. **10**

   (b) The frequency response of a filter has a form **10**

$$H(w) = e^{-3jw}\left[1 + 0 \cdot 4\cos 3w + 0 \cdot 2\cos 2w + 0 \cdot 2\cos w\right]$$

   Find the impulse response of the system.

7. Write short notes on (any **three**) :– **20**

   (a) Optimal linear phase FIR filter design
   (b) Discuss the design procedure of Bessel filter
   (c) Frequency transformation in digital domain
   (d) Chebyshev filter design
   (e) Design procedure of FIR filter design using Kaiser window
   (f) Quantization and limit cycle for first order and second order filter.

B.E (VII OLD) E&TC
Instrumentation System
7/12/2012

71 · 2nd half-12-(h) JP

Con. 8639-12. (OLD COURSE) KR–2403

(3 Hours) [Total Marks : 100

N.B.: (1) Question No. **1** is **compulsory**.
(2) Attempt any **four** questions out of remaining **six** questions.
(3) **Figures** to the **right** indicate **full** marks.

1. (a) How LVDT can be used for measuring linear as well as angular displacement ? **5**
(b) Explain PC based data acquisition system. **5**
(c) Derive the expression for strain guage factor. **5**
(d) Explain Absorption type torque measurement. **5**

2. (a) Derive the expression for step response of second order system. **10**
(b) Explain ultrasonic and electromagnetic flow meters. **10**

3. (a) Explain the concept of Virtual Instrumentation with its advantage, disadvantage and applications. **10**
(b) Explain capacitive and inductive type of transducers. **10**

4. (a) Explain digital data acquisition system and also give advantage of digital DAS over Analog DAS. **10**
(b) Differentiate based on principles of working materials used, different specification, advantages and disadvantages of RTD, Thermo couple and thermistor temperature transducers. **10**

5. (a) What are different materials used for strain gauges ? Explain different gauge circuits used in instrumentation system. **10**
(b) Short note on :— Data Logger. **10**

6. (a) Explain Hall effect with its use in displacement measurement. **10**
(b) Explain the characteristics of transducers and give the classification of transducers. **10**

7. (a) What different types of pressure sensors are used in instrumentation system ? Explain any one method. **10**
(b) Short note on : Piezoelectric Transducers. **10**

B.E (E TAR) VII OLD Dec-2012

Basic of VLSI

47-p3-d-upq-SH KSL12 C

Con. 10328–12. (OLD COURSE) KR–2484

(3 Hours) [Total Marks : 100

N.B. :(1) Question No. 1 is **compulsory**.
(2) Solve any **four** from remaining **six** questions.
(3) Assume **suitable** data if **necessary**.

1. (a) What is Velocity Saturation ? How does it affect the I–V characteristics of a short channel MOSFET. **5**
(b) Compare CMOS NAND with CMOS NOR gate which requires less area. **5**
(c) Compare Burried and Butting Contacts. **5**
(d) Draw stick diagram for CMOS inverter. **5**

2. (a) Calculate the threshold voltage V_{TO} at $V_{SB} = 0$, for a polysilicon gate N-Channel MOS transistor, with following parameters :— **10**

Substrate doping density $N_A = 10^{16}$ cm^{-3}

Polysilicon gate doping density $N_D = 2 \times 10^{20}$ cm^{-3}

Gate oxide thickness tox = 300 Å

Oxide interface fixed charge density $N_{OX} = 4 \times 10^{10}$cm^{-2}

(ni = 1·45 x 10^{10}/cm^3, εox = 0·345 x 10^{-12} F/cm^2

εsi = 1·035 x 10^{-12} F/cm^2)

(b) Explain the short channel effect with respect to the following points :— **10**
(i) Subthreshold conduction
(ii) Channel length modulation effect
(iii) Drain induced barrier lowering
(iv) Velocity saturation and mobility degradation.

3. (a) Describe various types of load which can be used for inverter gives their advantages and limitation. **10**
(b) Describe the limitation of a scaling of a MOS device. Derive the gate delay and power dissipation change after scaling in terms of scaling factor. **10**

4. (a) In the inverter circuit what is meant by Zpu/Zpd. Derive the required ratio between Zpu/Zpd if an n MOS inverter is to be driven from another inverter. **10**
(b) Implement the following Boolean function in CMOS logic. **10**

$$Y = \overline{A(D + E) + BC}$$

Draw the stick diagram for the circuit.

| TURN OVER

5. (a) Explain Ion implantation and compare it with diffusion clearly stating the advantages and disadvantages. 10

   (b) Draw the stick diagram and mask layout using λ based design rules for two i/p CMOS NAND gate with a pull up to pull down ratio as 4 : 1. 10

6. (a) Explain the latch up in CMOS. What are the remedies to avoid it. 10

   (b) Design 4 : 1 multiplexer using NMOS pass transistor. Also draw the stick diagram. 10

7. Write short notes on any **two** of the following :— 20

   (a) VHDL in VLSI design

   (b) Power dissipation in CMOS inverter

   (c) Photolithography in IC fabrication.

B E / I T R X VII (old) 12/12/12
Digital Communication

D Scan Pra I 10

Con. 10860-12. (OLD COURSE) KR-2637

(3 Hours) Total Marks : 100

N.B. (1) Question No. **1** is **compulsory**.
(2) Attempt any **four questions out** of remaining **six** questions.
(3) Assume any suitable **data if required.**

1. (a) The channel capacity is given by $C = B \log_2 \left(1 + \frac{S}{N}\right)$ in the presence of which gaussian noise with a constant signal power the channel capacity reaches its upper limit with increase in the bandwidth B. Prove that this upper limit of C is given by $C_\infty = 1{\cdot}44 \ S/N_o$. 10

(b) State and prove Central Limit Theorem. 10

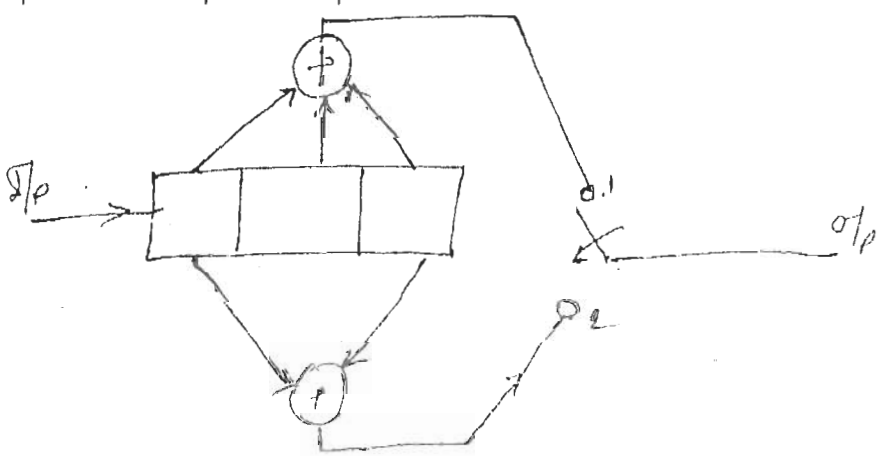
2. (a) Why is differential encoding used in PSK systems ? 5
(b) Explain the advantage of gray coding of the i/p to QPSK system. 5
(c) Differentiate source coding line coding and error delation codes. 10

3. Consider (7, 4) code whose generator matrix is– 20

$$G = \begin{bmatrix} 1 & 1 & 1 & 1 & 0 & 0 & 0 \\ 1 & 0 & 1 & 0 & 1 & 0 & 0 \\ 0 & 1 & 1 & 0 & 0 & 1 & 0 \\ 1 & 1 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}$$

(a) Find all the codewords of code.
(b) Find if the parity check matrix of the code
(c) Compare the syndrome for the received vector 1101101. is this a valid code vector ?
(d) What is the error correcting capability of the code ?
(e) What is the error delecting capability of the code ?

4. (a) A convolution encoder shown in **Figure** allows the shift of 2 message bits at a time what will be the constraint length and rate efficiency of the code. Initially consider that the register contains all zeros. What will be the code sequence if the i/p data sequence is 100110 ? 15



(b) Compare digital modulation techniques.

[TURN OVER

5. (a) What is offset and non offset QPSK explain indetail ? 10
   (b) What is inter symbol interference ? How does it a rise in a communication system ? Explain a system which will eliminate the same with the help of block diagram and with sketches. 10

6. (a) The Rayleigh density function is given by– 10

$$f(x) = \begin{cases} xe^{-x^2/2} & x \geq 0 \\ 0 & x < 0 \end{cases}$$

   (i) Prove that the f(x) satisfies fundamental properties of probability density function.
   (ii) Find the distribution function f(x).

   (b) Explain with neat block diag direct sequence spread spectrum technique. 10

7. Write short notes on :– 20
   (a) Processing gain
   (b) Jamming margin
   (c) Eye pattern
   (d) Viterbi decoding.

B.E (Electronics) Sem-VII (Old) Elective-I
Microcomputer System Design
17/12/12

p3-upq-Con-12--255

Con. 10990–12. (OLD COURSE) KR–3150

(3 Hours) [Total Marks : 100

- **Question Number 1 is compulsory. Solve any 4 from remaining 6 questions**
- **Draw neat diagrams wherever necessary.**

1. a. Explain any one Read Scenario explaining the MESI cache consistency model in the Pentium. (10)

b. Explain the reasons for the Green Nature of the PCI Bus. (10)

2. a. Explain with a neat diagram the Code cache organization of the Pentium. Explain the directory entry fields. (10)

b. Explain with a neat diagram a read transaction followed by a write transaction on the PCI bus. (10)

3. a. Draw State diagram of Pentium Bus cycles. Explain each state and cause for the transition. (10)

b. Explain the interrupts of the Pentium Processor. (10)

4. a. Explain SCSI Bus protocol in detail. (10)

b. Describe pipelined and non-pipelined bus cycles. in the Pentium (10)

5. a.Explain floating-point instruction execution stages in Pentium processor. (10)

b. Explain the following: i. Latency timer in PCI Bus. (10)
ii. Zone Bit recording in IDE

6. a. Explain in detail the function of the two prefetch queues in the Pentium processor. (10)

b. Explain IDE protocols. (10)

7. Write short notes on: (20)

a. CHS and LBA addressing in IDE.
b. USB transfers.
c. Plug and Play feature of PCI.
d. Split-Line Access mechanism in Pentium.

B.E(Electronics) Sem-VII (Old) Elective-I
Wireless communication
17/12/12

27 : 2nd half.12-shilpa(d)

Con. 8709-12. (OLD COURSE) KR-3168

(3 Hours) [Total Marks : 100

N.B. : (1) Question No. 1 is **compulsory**.
(2) Attempt any **four** questions out of remaining **six** questions.
(3) **Figures** to the **right** indicate **full** marks.

1. (a) What is frequency reuse concept ? 5
(b) Define reflection, diffraction and scattering, the three basic propogation mechanisms in mobile communication. 5
(c) Differentiate between fast fading and slow fading. 5
(d) Write a note on DECT. 5

2. (a) Explain multipath fading. What are the different physical factors which influences small scale fading ? 10
(b) For two-ray ground reflection model, derive the expression for received power, Pr (d) at a distance 'd' from the transmitter. 10

3. (a) Explain G.S.M. Architecture and give radio air interface specifications (for GSM). 10
(b) What are architectural methods for capacity expansion in cellular communications ? 10

4. (a) Describe knife edge Diffraction model with example. 10
(b) What are the features and services that has been standardized in cDMA ? 10

5. (a) Explain with neat diagram, the functions of each block in detail for signal processing in G.S.M. 10
(b) Explain speech channel coding and inter leaving used in USDC systems. 10

6. (a) If 20 MHz total spectrum is allocated for a duplex wireless cellular system and each simplex channel has 20 KHz RF bandwidth find :– 10
(i) The no. of duplex channels
(ii) The total no. of channel for cellsite if N = 4, cell reuse is used.
(b) Explain CDPD network Architecture. 10

7. Write short notes (any **four**) :– 20
(a) GSM Frame structure
(b) Cell dragging
(c) GPRS
(d) Subscriber Identity module
(e) CT2.
