BE | ETRX | VII (CBSGS) 26 | 11 | 12
Filter design

25 2nd half-12 (b) JP

Con. 8390-12. KR–1029

(3 Hours) [Total Marks : 100

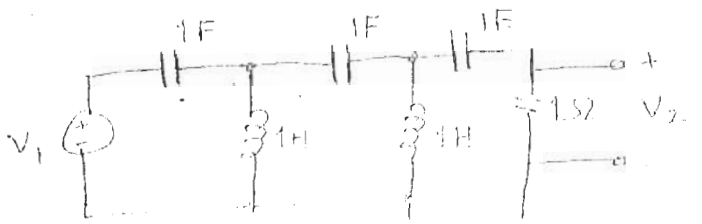
N.B.: (1) Question No. **1** is **compulsory**.
(2) Attempt any **four** questions from remaining **six** questions.
(3) Assume **suitable** data wherever **necessary**.

1. (a) Give difference between Butterworth. Chebyshev and elliptic filters. **5**
(b) Describe basic principles of working of switched capacitor filter with example. **5**
(c) What is adaptive filter, explain with the help of suitable example. **5**
(d) Explain multirate signal processing. Why antialiasing / antiimaging filter required ? **5**

2. (a) Design an analog bandpass filter for following specificatios :— **15**
(i) Passband 200 rad/s – 800 rad/s
(ii) Stopband 0 rad/s 100 rad/s and
1600 rad/s onwards
(iii) Passband attenuation 3dB
(iv) Stopband attenuation 10 dB
(v) Chebysher filter.
(b) Explain basic Weiner filter. **5**

3. Design a Butterworth, digital lowpass filter for following specifications. Plot pole-zero plot also. Use bilinear transformation (BLT) method : **20**
(i) Passband 0 – 1 KHz
(ii) Stopband 3 KHz – onwards
(iii) Passband attenuation 2·3 dB
(iv) Stopband attenuation 18 dB
(v) Sampling frequency 12 KHz
(vi) Low-pass filter
(vii) Plot pole-zero plot of analog filter only.

4. (a) What is inductance simulation. explain. **5**
(b) Realize/synthesize following passive network using synthetic (simulated) inductor. **5**



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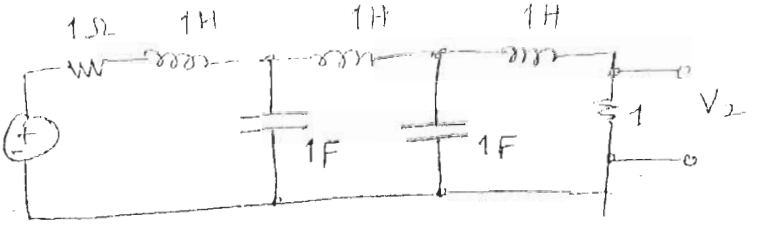
(c) Explain Leap frog realization technique with suitable example. 5

(d) Realize following passive network using FDNR (frequency dependent negative resistor). 5



5. (a) Design a FIR filter for $\delta_p = 0{\cdot}01$, $\delta_s = 0{\cdot}1$, $W_p = 0{\cdot}2$, $W_s = 0{\cdot}6$ using any suitable window. 10

(b) Design a frequency sampling filter for following specification $|H(k)| = \{1, 1, 0, 0, 0, 1\}$. 10

6. (a) For i\p sampling rate of 50 KHz and output sampling rate of 1 KHz, give 2-stage decimation scheme. Compare the filter order required for antialising filters of two stage implementation with single single stage implementation. Comment on the results. 10

(b) Explain with suitable example polyphase interpolation. comment/compare with single phase interpolation. 10

7. Write short notes on (a) and (b). Attempt any **three** :

(a) MMSE criterion in adaptive filter 6

(b) LMS and RLS algorithm in adaptive filtering 7

(c) Design an active lowpass, second order filter for $W_n = 1$ KHz and $Q = 0{\cdot}707$. 7

(d) What is subband conding and quadrature mirror filtering, explain. 7

Con. 9722-12. (REVISED COURSE) **KR-1152**

(3 Hours) [**Total Marks : 100**

N. B. : (1) Question No. 1 is **compulsory**.
(2) Attempt any **four** questions out of remaining **six** questions.
(3) **Figures** to the **right** indicate **full** marks.
(4) Assume **suitable** data wherever **required** but justify it.

1. Answer the following :— 20
   (a) Discuss the effect of source-inductance on the performance of a single phase fully controlled converter.
   (b) Explain continuous conduction mode and discontinuous conduction mode of class A chopper.
   (c) Compare between current source and voltage source inverters.
   (d) List the advantages offered by DC Chopper drives over line commutated conveter controlled d·c· drives.

2. (a) Explain sinusoidal pulse modulation as used in PWM inverter. 10
   (b) A capacitor commulated single phase bridge inverter is operated at 50 Hz with load resistance of 5 ohm. thyristor turn-off time is 62 μ sec. 10
   Determine :
   (i) Commutating capacitor C for successful commutation of SCR.
   (ii) Load current I_L.
   (iii) F critical for reliable commutation.
   (iv) R critical.

3. (a) Draw and explain the operation of single phase capacitor commutated current source invertor with resistive load. Draw also and related voltage and current waveform. 10
   (b) What are the disadvantages of harmonics present in the inverter circuit. List the methods of harmonic reduction in Inverters and explain any one method in detail. 10

4. (a) Draw and explain the operation of a speed control of a d·c· series motor by a single phase semiconverter for the continuous motor current. Draw also the associated current and voltage waveforms. 10
   (b) A d·c· shunt motor takes a current of 80 A on a 480 V supply and runs at 960 rpm, the armature resistance is 0·25 ohm and the field resistance is 120 ohms. A Chopper is used to control the speed of the motor in the range of 400-750 rpm having constant torque. The ON period of the chopper is 3 ms. The field is supplied directly from 480 V supply. Determine the range of frequencies of the chopper. 10

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5. (a) Explain the operation of induction motor for two different cases when fed by current source inverter :— 10
   (i) Operation at and below rated frequency
   (ii) Operation above rated frequency.
   (b) Discuss the stator voltage control scheme of Induction motor. Also draw and explain the speed torque curves. 10

6. (a) Describe the operation of on-line UPS system with the help of neat block diagram. Also list the important specifications of on-line UPS. 10
   (b) With the help of neat circuit diagram explain the working of SMPS. 10

7. Write short notes on the following :— 20
   (a) Dual Converter
   (b) Mc Murry Inverter
   (c) Series Inverter.

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Sub:- VLSI Design.

ws Sept, 2012 (b) 120

Con. 8407–12. **KR–1269**

(3 Hours) **[Total Marks : 100**

N. B. : (1) Question No. **1** is **compulsory**.
(2) Solve any **four** questions from remaining **six** questions.
(3) Draw **neat** diagrams and assume **suitable** data if **required**.

1. (a) Write equations and draw the profile for diffusion from constant source and diffusion from instantaneous source. **5**
   (b) Draw VTC of three CMOS inverter circuits (on smae Plot) with $K_R = 1$, $K_R < 1$ and $K_R > 1$. **5**
   (c) Draw the profile inidcating sub-threshold conduction in MOSFET and show ideal value of sub-Threshold slope on it. **5**
   (d) A microprocessor was fabricated in a 0·25 μm technology and was able to operate at 100 MHz, consuming 10 watt using a 2·5 V power supply. **5**
      (i) Using fixed voltage scaling, what will the speed and power consumption of the same processor be if scaled to 0·1 μm technology ?
      (ii) If the supply voltage on the 0·1 μm part were scaled to 1·0 V, what will the power consumption and speed be ?

2. (a) With device cross section and band diagram, discuss accumulation, depletion and inversion in MOS capacitor. **10**
   (b) Find the depletion layer width X_d the depletion region charge Q_{BO}, The throshold voltage with no source to body voltage V_{Tho} and the body factor Y of a device with the following physical parameters : **10**

   $T_{ox} = 400°A$,
   $N_A = 1·5 \times 10^{16}$ cm^{-3},
   $N_D = 10^{18}$ cm^{-3},
   N_{SS} (density of singly charged positive surface ions) $= 5 \times 10^{16}$ cm^{-2}.

3. (a) What is the necessity of design rules ? Specify lambda based design rules ? Draw CMOS inverter for $(W/L)_p = 3(W/L)_N$ with design rules (indicate scale in terms of lambda on layout). **10**
   (b) What is latch-up in CMOS ? How to provent latch-up in CMOS ? **10**

4. (a) Calculate noise margin for the CMOS invertor with the following specifications : **10**

   $V_{DD} = 5$ V, $V_{To, n} = 1·0$ V, $V_{To, p} = -1·2$ V, $K_n = 100$ μA/V^2, $K_p = 40$ μA/V^2. **10**
   (b) Derive an expression for calculation of V_{OL} and V_{IL} for CMOS inverter.

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5. (a) Design the circuit and draw layout for the function $Y = \overline{(D + E + A)(B + C)}$ using CMOS logic. Also find equivalent CMOS inverter circuit for simutaneous switching of all inputs assuming That $(W/L)_p = 15$ for all PMOS transistors and $(W/L)_n = 10$ for all NMOS transistors. **10**

   (b) Draw cross section diagrams and their corresponding masks for all important masking steps required for fabrication of CMOS inverter with n-well process. **10**

6. (a) Implement 2:1 multiplexer circuit using CMOS transmission gates and write switch level verilog HDL model for it. **10**

   (b) Implement CMOS 1-bit full adder and write gate level verilog HDL module for it. **10**

7. Write short notes on any **four** :– **20**
   (a) Y-chart representation for VLSI design
   (b) Dry and wet oxidation process
   (c) Transistor sizing
   (d) Bulting and Buried contacts
   (e) Short channel effects.

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Con. 10838-12. **(REVISED COURSE)** **KR–1485**

(3 Hours) **Total Marks : 100**

N. B. (1) Question No. 4 is **compulsory**.
(2) Solve any **four** questions from the remaining.
(3) Assume **suitable** data wherever **required**.

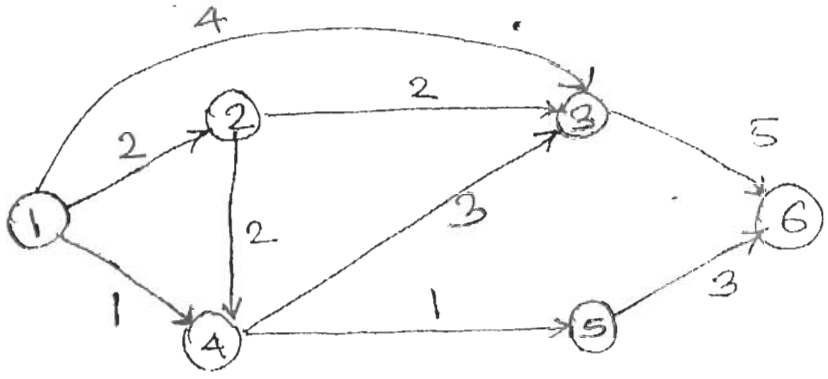
1. (a) What is difference between Network layer delivery and transport layer delivery ? **20**
   (b) What is difference between congestion control and flow control ?
   (c) In sliding window flow control method why size of window is one less than the modulo range ?
   (d) What are the conditions to be satisfied for valid CRC generator polynomial ? Draw block diagram of CRC generator.

2. (a) Explain CSMA/CD and its use. What part of 802 project uses CSMA/CD ? **10**
   (b) Explain Repeates, Bridges, Routers and Switches. **10**

3. (a) Explain HDLC protocol with frame format. **10**
   (b) Explain ADSL in detail. **10**

4. (a) What is extirier and interior routing ? Explain in brief path vector routing and distance vector routing. **10**
   (b) Explain ISDN channel structure for basic and primary services. **5**
   (c) Explain Berkley API. **5**

5. (a) Apply Djkstra and Bellman Ford algorithm to given network and find the least cost path between source node 1 to other nodes. **12**



   (b) Compare circuit switching, packet switching and Virtual circuit packet switching. **8**

6. (a) Explain LAN protocol architecture with IEEE 802 reference. Sketch the general MAC frame format and LLC PDU structure. Explain the functions of different fields. **10**
   (b) Explain SONET/SDH in detail. **10**

7. (a) Explain SMTP and HTTP. **5**
   (b) Explain bit stuffing. **5**
   (c) How does reservation work with medium access control ? **5**
   (d) Discuss various network topologies. **5**

BE-Electronics - Sem - VII (REV COURSE) Elective - I
Digital Image Processing Design
17/12/12

ws-Con-2012

Con. 10909–12. **(REVISED COURSE)** **KR–1863**

(3 Hours) **[Total Marks : 100**

N.B. : (1) Question No. **1** is **compulsory**.
(2) Assume **suitable** data wherever **necessary**.
(3) Attempt any **four** questions from remaining questions.

1 State true or false and justify (Any Four): **20**

(a) Poorly illuminated images can be easily segmented.
(b) All Image Compression techniques are invertible.
(c) Chain Codes can be made invariant to translation and rotation.
(d) The principal operation of median filter is to force points with distinct intensities to be more like their neighbors.
(e) Quality of the picture depends on the number of pixels and the number of gray level that represent the picture.

2 (a) An image represented by 8 bit/pixel has following gray level distribution. Perform histogram equalization and give new distribution of gray level. **10**

Gray Level	0	1	2	3	4	5	6	7
Number of pixels	128	75	280	416	635	1058	820	684

(b) Explain Segmentation based on discontinuity and similarity **10**

3 (a) Obtain Huffman Code for the word "COMMITTEE" **10**

(b) Explain Homomorphic filtering. **10**

4(a) What are the different types of redundancies in an image? Explain how they can be reduced / eliminated. **10**

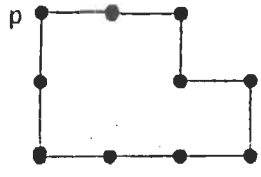
(b) List any two properties of 2D DFT and prove any one of them. **10**

5 (a) Apply the following Image Enhancement techniques on the given Image. **10**

(i) Digital Negative (ii) Bit Plane Slicing (iii) Thresholding

2	1	3	7	4
4	5	2	0	1
3	5	1	4	6
0	4	0	2	3
2	1	6	1	4

(b) Obtain the 4 Directional Chain code for the image shown below. Find first Difference and circular first difference. **10**



6 (a) For 2x2 transform A and the image U, Compute Transformed image V and the basis image **10**

$$A = \frac{1}{\sqrt{2}}\begin{bmatrix} 1 & 1 \\ 1 & 1 \end{bmatrix}, \quad U = \begin{bmatrix} 1 & 2 \\ 3 & 4 \end{bmatrix}$$

(b) Give following masks of size 3×3 and explain their usefulness in image Processing. (i) Sobel (ii) Roberts (iii) Low-pass filter (iv) Prewitt (v) Laplacian **10**

7 Write short notes (**Any Four**) **20**

(i) Dilation and erosion
(ii) Image Sampling
(iii) JPEG
(iv) Connectivity of pixels
(v) Filtering in Frequency domain