BE. ETRX Sem-7. (Rev) 5/12/13

16-11-13-DTP7-RM-22

Power Electronics & Drives

Con. 8713-13. **LJ-14047**

(Revised Course)

(3 Hours) **[Total Marks : 100**

N.B. : (1) Question No. 1 is **compulsory.**

(2) Attempt any **four** questions out of remaining **six** questions.

(3) **Figures** to the **right** indicate **full** marks.

(4) Assume **suitable** data if **required** but justify the **same**.

1. Attempt the following :-

(a) Why voltage control is needed in inverter circuit? State the various methods of voltage control in inverter circuits. **20**

(b) In a single phase full converter the reduction in the output voltage due to the effect of source inductance is 3 Volts. The load current is continuous and ripple free and equal to 100 Amp. Find the value of source inductance and overlap angle if supply voltage is 230V, 50 Hz and $\alpha=\frac{\pi}{6}$.

(c) Explain the 'Pluggeing' for D.C. motors.

(d) A step up chopper has output voltage of 2 to 4 times the input voltage. For a chopping frequency of 2000 Hz, determine the range of off periods for the gate signal.

2. (a) Explain the working of two quadrant type B chopper with the help of neat circuit diagram and waveforms. **10**

(b) Explain volts/hertz control for a 3 phase induction motor for its speed control. Emumerate its advantages. **10**

3. (a) Explain the operation of Dual Converter with neat circuit diagram and waveforms, and give the comparison between non circulating and circulating current mode. **10**

(b) With the help of neat circuit diagram and waveforms, explain the operation of single phase capacitor commutated current source inverter with R load. **10**

4. (a) Draw and explain the power circuit of semiconverter feeding a separately excited D.C. motor. Explain with typical voltage and current waveforms, the operation in both continuous and discontinuous current mode. **10**

(b) Derive the expression for commutating components L and C for a voltage commutated chopper. Also discuss the assumptions made for designing the components. **10**

[TURN OVER

5. (a) Explain the operation of basic series inverter and draw the waveforms for **10**
   (i) Voltage across the capacitor
   (ii) Voltage across the inductor
   (iii) Voltage across the load resistance
   How will you modify it so that the supply current flows in both the half cycles of output voltage ?
   (b) Explain with neat diagram and waveforms, the operation of half bridge switching regulator. **10**

6. (a) Describe static rotor resistance control method for the speed control of a 3 phase induction motor. Show the effect on developed torque and stator current. **10**
   (b) A separately excited D.C. motor is supplied from 230 V, 50 Hz source through a single phase half wave controlled converter. Its fild is fed through single phase semiconverter with zero degree firing angle delay. Motor resistance Ra = 0.7Ω and Motor constant = 0.5 V-sec/rad. For rated load torque of 15Nm at 1000 rpm and for constant ripple free current, determine. **10**
   (i) Firing angle delay of the armature converter.
   (ii) RMS value of thyristor current.
   (iii) Input power factor of the armature converter.

7. Write short notes on :- **20**
   (a) Offline UPS system.
   (b) Need for reduction of Harmonics in inverters.
   (c) Slip power recovery scheme.

SEM VII VLSI DESIGN NOVEMBER-DEC 2013

E-IRX

6051, 609

2nd Half-13(10)-PKL-68

Con. 9100-13. **LJ-14117**

(REVISED COURSE)

(3 Hours) **[Total Marks : 100**

N. B. : (1) Question No. **1** is **compulsory**.
(2) Attempt any **four** questions from remaining **six** questions.
(3) Assume suitable data, wherever required.

1. Answer any **four**:– **20**

(a) Consider a MOS capacitor made on a p-ytpe substrate with doping of $10^{16}/cm^3$. The SiO_2 thicknessis 500 A° and the metal gate is made of aluminium. Calculate the minimum capacitance at threshold.

(b) An NMOS with V_T of 1.5 V is operated at V_{GS} = 5 V and I_{DS} = 100 μA. Determine if the device is in linear or saturation regime. Assume that K = 20 $\mu A/V^2$.

(c) Consider a resistive load NMOS inverter with the output voltage 0.2 V when the input is $V_{OH} = V_{DD}$ = 5 V. Find the DC power dissipation of the circuit.

(d) "Two critical voltage points on the voltage transfer characteristics of a realistic inverter are identified at points where the slope of the V_{out} (V_{in}) characteristic becomes equal to –1." Justify the selection of these critical voltage points based on noise considerations.

(e) Explain the layout design rule for minimum gate extension of polysilicon over active and the problems faced in case of violation of the rule during fabrication. Draw appropriats diagrams.

2. (a) Explain the various parameters affecting the threshold voltage of a MOS structure. Also explain the influence of substrate bias and ion implantation (in the channel region) on the threshold voltage of the device. **10**

(b) Consider an n-channel MOSFET at 300K with the following parameters:– **10**

Channel length, L = 1.5 μm , channel doping, Na = $1\times10^{16}/cm^3$
Channel width, W = 25 μm , Oxide thickness, tox = $500A^0$
Channel mobility, μn = 600 $cm^2/v\text{-}s$, Oxide charge Q_{SS} = $10^{11}/cm^2$
Metal - SC work function difference , ϕms = –1.13 V.
Calculate the saturation curent of the device at a gate bias of 5 V.

3. (a) Derive an expression for the switching voltage of a CMOS inverter. Design the CMOS inverter with a switching voltage of $\frac{V_{DD}}{2}$. **10**

(b) Draw the schematic and stick diagram of a 2-input CMOS NOR gate and determine the sizes of the transistors such that it has approximately same t_{PLH} and t_{PHL} as an inverter with the following sizes: **10**

$$\left(\frac{W}{L}\right)_{NMOS} = \frac{0.5\mu m}{0.25\mu m} \text{ and } \left(\frac{W}{L}\right)_{prnos} = \frac{1.5\mu m}{0.25\mu m}$$

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4. (a) Design a two input NAND gate in NMOS technology based on a reference nMOS depletion load inverter with inverter ratio, $k_R = 4$. Draw the stick diagram and the mask layout of the circuit designed following the λ based design rules. 10

   (b) Compare the passive and active loads used in an nMOS inverter circuit stating their advantages and disadvantages. 10

5. (a) Explain the basic sequence for building a self-aligned p-channel MOSFET with the help of appropriate diagrams. 10

   (b) Implement circuit for 2:1 multiplexer using transmission gate logic and write verilog module for the circuit designed. 10

6. (a) Compare and explain the effect of full scaling and constant voltage scaiing on MOSFET dimensions, potentials, doping densities and other key device characteristics. 10

   (b) Implement the following Boolean function in CMOS logic. 10

$$Y = \overline{(A+D+E)\,(C+B)}$$

Drow the stick diagram of the circuit and find an equivalent CMOS inverter circuit for simultaneous switching of all inputs, assuming that $\left(\frac{W}{L}\right)_P = 15$ for all PMOS transisters and $\left(\frac{W}{L}\right)_n = 10$ for all nmos transisters.

20

7. Attempt any **two**:–

   (a) CMOS latch-up and its prevention

   (b) MOS CV characteristics

   (c) Short channel effects.

B.E (ETRx) Sem VII
Comm. Networks

17/12/13

25-11-13-DTP7-RM-9

Con. 9688-13.

LJ-14234

(Revised Course)
(3 Hours)

[Total Marks : 100

N.B. : (1) Question No. **1** is **compulsory**.
(2) Answer any **four** questions out of remaining **six** questions.

1. Answer briefly (any **four**) :- **20**
   (a) What is meant by data transparency ? How is it implemented in HDLC protocol ?
   (b) What is the difference between congestion control and flow control ?
   (c) Explain various network Topologies
   (d) Compare OSI model with TCP/IP model.
   (e) List and explain functions of Data Link Layer.

2. (a) Explain OSI Rreference Model architecture for a network with two intermediate nodes, with a neat diagram. Also explain the functions of each layer. Name the layers responsible for (i) end to end reliability and (ii) link to link reliability. **8**
   (b) What is meant by flow control ? Discuss the different flow-control methods with neat diagrams. **8**
   (c) Explain different ARQ techniques. **4**

3. (a) Explain ADSL with respect to channel configuration and modulation technique. **8**
   (b) What are transmission impairments ? Explain. Compare Co-axial cable, optical fiber cable with respect to transmission characteristics, data rate and bandwidth, applications. **8**
   (c) List the categories of UTP cables. How is noise-interference minimized in twisted pair cables ? **4**

4. (a) With respect to HDLC Protocol, explain the following :- **10**
      (i) HDLC frame format.
      (ii) Different HDLC frames.
      (iii) Data transfer modes.
      (iv) Balanced and unbalanced configurations.
      (v) Importance of P/F bit.
      (vi) 'Polling' Technique and 'Select' routine.
      (vii) Flow control and error control commands.
   (b) Sketch the appropriate HDLC frames for the following scenario involving Primary station 'A' and two Secondary stations B and C. **10**
      (i) Primary station 'A' wishes to establish a Normal Response mode-link with secondary stations B and C.
      (ii) Both the stations B and C, send positive acknowledgements to A.
      (iii) Station 'A' sends a polling command to 'B' and 'B' sends 3 data frames. A sends positive-Ack to indicate the receipt of error-free data frames.
      (iv) Station 'A' sends a 'select' command to 'C'. When 'C' responds with 'ready' response, 'A' sends 3 data frames to C and C sends positive-Ack to indicate the receipt of error-free data frames.
      (v) What is Piggybacking ? Give an example of Piggybacked frame.

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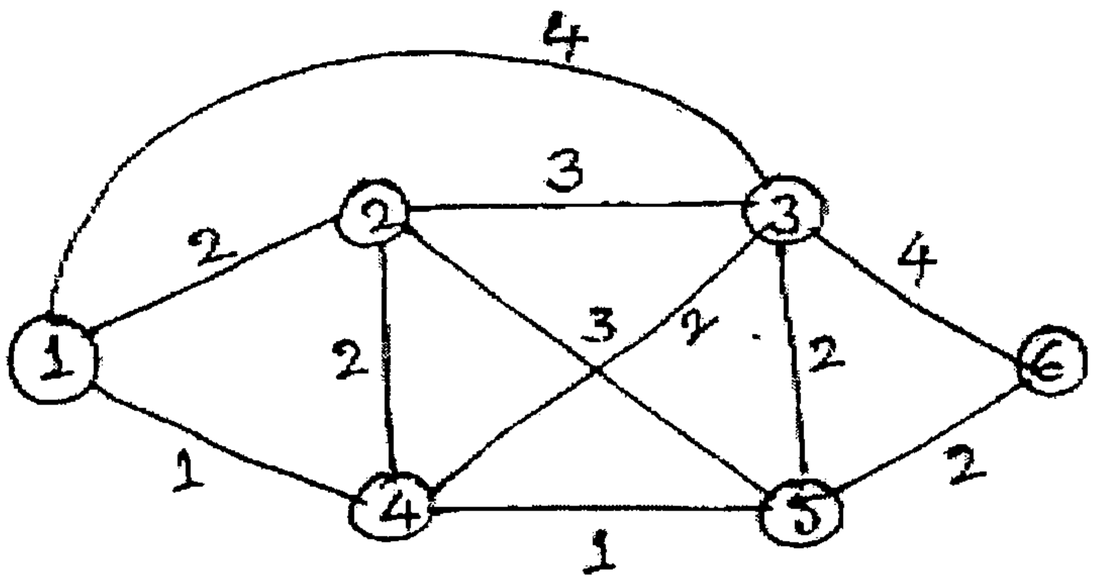
5. (a) What is meant by 'blocking' in space-div-switching ?
   (i) Derive the condition required to make 3-stage space-div-switch to be a non-blocking switch. **4**
   (ii) Sketch a 3-stage space-div-switch and TST switch with N = 16, n = 4 and K =3. **6**
   (iii) Show how blocking occurs in the above 3-stage space-div-switch diagram. **2**

   (b) Draw a diagram of packet-switched network and explain how virtual-circuit packet switching works. And compare circuit-switching, datagram switching and virtual-circuit packet switching. **8**

6. (a) Apply Djikstra's and Bellman-Ford Routing algorithms to given network and find the least cost path from source node-1 to all other nodes. [**Note** : steps of algorithms must be written.] **12**



   (b) Explain LAN Protocol architecture with IEEE 802 reference. Sketch the general MAC frame format and LLC-PDU structure. Explain the functions of different fields. **8**

7. (a) Explain the functions of different connecting devices :- Repeaters, Bridges, Routers and Switches. **8**
   (b) Write short notes on (any **three**) :- **12**
   (i) ISDN
   (ii) Congestion control Techniques.
   (iii) Spanning tree algorithm.
   (iv) Token-Reinsertion strategies.
   (v) Routing Strategies for Packet Switching.

BE. ETRX - Sem 7 25/11/Nov 13

11-11-13-DTP6-MU-12

Filter Design

Con. 7767-13. **LJ-13915**

(Revised Course)

(3 Hours) **[Total Marks : 100**

N.B. : (1) Question No. **1** is **Compulsory**.
(2) Answer any **four** questions out of remaining **six** questions.
(3) Assume **suitable data** if **necessary**.

1. (a) Compare FIR and IIR filters. **20**
(b) Sketch the characteristic response of Butterworth, Chebyshev - I and II, and elliptic filters in analog domain.
(c) Ideal filter characteristics are not realisable. Give reason for the same.
(d) Describe the basic principle and writing of switched capacitor filter.
(e) Digital the analog transfer fortune using impulse invariable method.

$$H_a(s) = \frac{2}{(s+1)(s+3)}$$

2. (a) Prove that zeros points of a linear phase FIR filter occur at reciprocal locations. **5**
(b) Design a low pass IIR Butterworth filter for the following specifications. **15**
(i) Passband attn = 1dB
(ii) Stopband attn = 15 dB
(iii) Passband edge frequency = 200 Hz
(iv) Stopband edge frequency = 540 Hz
(v) Sampling frequency = 8 KHz
Use Bilinear transformation.

3. (a) Design a low pass linear phase FIR filter for 11 coefficient using Hamming window for following specifications. **10**
Passband frequency : 0.25 KHz
Sampling frequency : 1 KHz
(b) Derive the expression for order N of Butterworth filter. **10**

4. (a) Prove that $S=\frac{2}{T}\left(\frac{1-Z^{-1}}{1+Z^{-1}}\right)$ and $w=2\tan^{-1}\left(\frac{\Omega T}{2}\right)$, in Bilinear transformation method. **10**
Explain the mapping between analog and digital frequency to domains.
(b) Explain frequency sampling technique of FIR filter design. **10**

5. (a) What is FDNR? State and explain its properties and method to realine a low pass filter using FDNR. **10**
(b) Explain the effect of interpolation and decimation in time and frequency domain. **10**

[TURN OVER

6. (a) Write a note on the frequency transformation technique of converting a normalized low pass filter into the desired one. **10**

   (b) Compare frequency mapping in impulse invariance and Bilear transformation method. **10**

7. Write short notes on (any **three**):– **20**

   (i) Adaptive filter. characteristics

   (ii) Window functions - chola response and features.

   (iii) Sub-bond coding technique.

   (iv) FIR filter design using Kaisee window.

Digital Image Processing Design.
Sem VII ETRX 30/11/13

14-11-13-DTP-P-14-AK-20

Con. 8482-13. **LJ-13990**

(Revised Course)

(3 Hours) **[Total Marks : 100**

N.B. : (1) Question No. **1** is **compulsory**.
(2) Solve any **four** questions from the remaining **six** questions.
(3) Assume **suitable** data if **needed**.

1. Justify any **four** of the following statements :- **20**
   (a) Reduction in spatial resolution results in checker board degradation.
   (b) Huffman coding is a lossless compression technique.
   (c) Butterworth lowpass filter is preferred to ideal lowpass filter.
   (d) It is difficult to segment poorly illuminated images.
   (e) Dynamic range compression is used in displaying the Fourier transform of an image.

2. (a) The gray level distribution of an image is shown in the table below. Perform histogram equalization and plot the original and equalized histograms. **10**

Gray level	0	1	2	3	4	5	6	7
Frequency of occurrence	0	50	100	200	400	200	50	0

   (b) With the help of block diagram, explain the working of a Homomorphic filter. **10**

3. (a) A 5x5 image segment is shown below. Perform bitplane slicing and lowpass filtering on the same :- **10**

6	7	6	6	7
0	0	0	1	2
1	1	1	2	3
4	5	5	4	2
6	6	6	7	7

   (b) With the help of suitable examples, explain the following morphological operations :- **10**
      (i) Dilation
      (ii) Erosion.

4. (a) What are the different types of data redundancies found in digital images ? Explain in detail. **10**

[TURN OVER

(b) A source emits six symbols with probabilites as shown in the table below. Construct the Huffman code and calculate the coding efficiency. **10**

Symbol	a_1	a_2	a_3	a_4	a_5	a_6
Probability	0.05	0.25	0.05	0.15	0.2	0.3

5. (a) Obtain the 2DDFT of the image segment shown below using any one fast algorithm. **10**

$$f(x,y)=\begin{bmatrix}0 & 0 & 1 & 1\\ 1 & 2 & 0 & 0\\ 1 & 0 & 1 & 1\\ 2 & 0 & 1 & 0\end{bmatrix}$$

(b) What is Segmentation ? With the help of examples, explain segmentation based on similarity. **10**

6. (a) Explain the following with examples :- **10**
   (i) Signature
   (ii) Fourier Descriptor.

(b) State and prove periodicity and translation properties of 2DDFT. Write the transformation matrices for Hadamard and Fourier transforms for N = 4. **10**

7. Write short notes on any **four** :- **20**
   (a) Isopreference cuvers
   (b) Hough transform
   (c) Digital Water marking
   (d) Chain codes
   (e) Biometric Authentication.