BE ETRX Sem [illegible]

PE & Drives

3/12/14.

QP Code : 15418

(3 Hours) **[Total Marks : 100**

N. B. : (1) Question No. **1** is **compulsory**.
(2) Attempt any **four** questions out of remaining **six**.
(3) **Figures** to the **right** indicate **full** marks.
(4) Assume suitable data if required but justify the same.

1. Attempt the following :– **20**
   (a) How a constant v/f control is superior to the stator voltage control?
   (b) Give the performance comparison of VSI and CSI.
   (c) Discuss the different factors for selection of battery for UPS.
   (d) Give the comparison between dual converter operating in non circulating and circulating current mode.

2. (a) With the help of circuit diagram and associated waveforms, explain the principle of operation of type C chopper. **10**
   (b) Explain multiple pulse width modulation as used in PWM inverters. **10**

3. (a) Explain with neat diagram the slip power recovery technique to control the speed of 3 phase slip ring induction motor above and below the synchronous speed. State the advantages of this technique. **10**
   (b) Explain with neat diagram and waveforms the operation of flyback converter. **10**

4. (a) A separately exicted D.C. motor operating from a single phase half controlled bridge rectifier at a speed of 1400 rpm. has an input voltage of 330 sin 314 t and a back emf of 80V. The SCR's are fired symmetrically at $\alpha = 30°$ in every half cycle and the armature has a resistance of 4 Ω. Calculate the average armature current and the motor torque. **10**
   (b) Discuss the working of load commutated chopper with associated voltage and current waveforms. Show voltage variation across each pair of SCR's as a function of time. **10**

5. (a) Explain with neat diagram and waveforms the working of parallel inverter. What is the need for feedback diodes and pulse train for firing of SCR's. **10**
   (b) Discribe the working of a single phase full converter fed separately excited D.C. motor with circuit diagram, relevant waveforms and expressions. **10**

6. (a) Explain with neat diagram the static rotor resistance control method for the speed control of 3 phase induction motor. **10**

(b) Explain the effect of source inductane on the performance of a single phase fully controlled converter and derive the expression for the output voltage. 10

7. Write short notes on (any **two**) :–
   (a) Control strategies employed in chopper for operating the switches. 6
   (b) IR compensation 7
   (c) Mc Murry. inverter. 7

Elective - II

B.E. - Electronics. Sem VII Rev 13351

Wireless Comm 27/11/2014

QP Code : 15351

(3 Hours) **[Total Marks : 100**

N.B. : (1) Question No. **1** is **compulsory.**
(2) Solve any **four** questions out of remaining **six** questions.
(3) **Figures** to the right indicate **full** marks.
(4) Solve **one** complete question together.

1. (a) Explain the need of RAKE receiver in multipath propagation. **5**
   (b) Differentiate between soft hand-off and hard-hand off. **5**
   (c) Draw and explain block diagram for OFDM. **5**
   (d) Differentiate between IS-95 CDMA and CDMA 2000. **5**

2. (a) Draw and explain GSM frame structure in detail. **10**
   (b) Explain the different techniques to improve coverage area and capacity in mobile communication. **10**

3. (a) Draw and explain CDMA 2000 layered structure. **10**
   (b) Explain power control mechanism in IS-95 system. **10**

4. (a) Draw block diagram for signal processing in GSM. Explain it in detail. **10**
   (b) Differentiate between dynamic and fined channel assignment technique. **5**
   (c) Define Grade of service and traffic in intensity related to trunking theory. **5**

5. (a) With the help of block diagram, explain direct sequence spread spectrum. **10**
   (b) With the help of block diagram explain forward IS-95 CDMA system. **10**

6. (a) Explain different physical and logical channels in IS-95 system. **10**
   (b) Draw and explain GSM system architecture in detail. **10**

7. Write short notes on (any **two**) :—
   (a) Security in GSM. **10**
   (b) Data services in CDMA 2000 **10**
   (c) Zigbee Network. **10**

Elective II Elective ... 29/11/2014

BE
Sem VII

Digital Image Processing System

QP Code :15360

(3 Hours) **[Total Marks : 100**

N.B : (1) Question No. 1 is **compulsory**.
(2) Out of the remaining questions attempt any **four**.
(3) **Figures** in the **right** indicate maximum **marks**.

1. Answer any **four** :
   (a) Differentiate between spatial and tonal resolutions. **5**
   (b) Why is the sum of coefficients of a high pass filter mask zero? **5**
   (c) Compare Huffman coding and arithmetic coding; **5**
   (d) Give 3x3 masks for Laplacian filter, horizontal, vertical, $+45^0$ and -45^0 line detectors. **5**
   (e) Explain dilation and erosion in brief. **5**

2. (a) Explain the following enhancement operations and draw the graph of transformation function : **10**
   (i) Clipping, (ii) Bit plain slicing
   (b) Perform histogram equalization on the following image histogram and plot original and equalized histograms. **10**

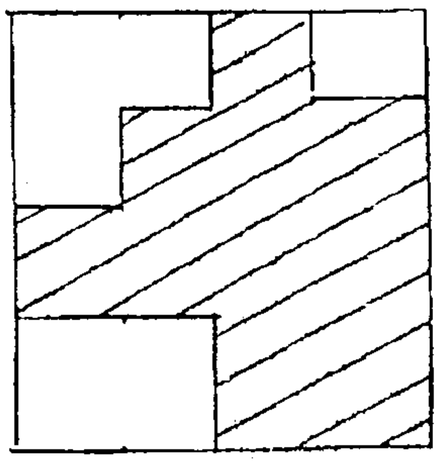
Gray Level	0	1	2	3	4	5	6	7
Number of pixels	200	300	500	350	250	0	0	0

3. (a) A source emits 6 symbols with the following probabilities : **10**

Symbol	A	B	C	D	E	F
Probability	0.1	0.2	0.05	0.05	0.35	0.25

Construct the Huffman code. Calculate the average code word length and coding efficiency.

(b) Perform region splitting and merging on the image segment shown below. Draw the quad tree. Briefly explain the method used. **10**



4. (a) Calculate the Hadamard transform of the image segment. 5

$$f(x,y)=\begin{bmatrix}2 & 3 & 1 & 4\\ 2 & 1 & 1 & 4\\ 1 & 3 & 4 & 4\\ 3 & 3 & 2 & 2\end{bmatrix}$$

(b) State and prove any two properties of 2DDFT. 5

(c) Obtain the 16 basis images of Hadamard transform. 10

5. (a) Given the 8 x 8 image segment, perform erosion using the structuring element shown: 10

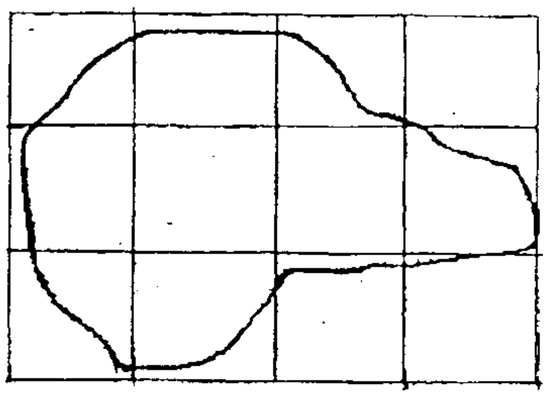
1	0	0	0	0	0	0	1
1	1	0	0	0	0	1	1
1	1	1	0	0	1	1	1
1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1
1	1	1	0	0	1	1	1
1	1	0	0	0	0	1	1
1	0	0	0	0	0	0	1

Structuringelement :

1	1
1	1

(b) With the help of a neat block diagram, explain the working of the homomorphic filter. 10

6. (a) What are chain codes? Obtain 4 connected and 8 connected chain codes for the boundary shown below: 10



(b) Explain in detail different types of data redundancies present in the digital images. 10

7. Write short notes on any four of the following: 20
   (a) Opening and closing
   (b) Color models
   (c) Finger print recognition
   (d) Digital water marking
   (e) Handwritten character recognition.

B.E Electronics Sem VII Rev 15357

Electn MSD 27-11-2014

QP Code : 15357

(3 Hours) **[Total Marks : 100**

N.B : (1) Question No **1** is **compulsory.**
(2) Solve any **four** from remaining **six** questions.
(3) Draw neat diagram wherever **necessary.**

1. (a) Explain organization of data cache of Pentium processor and explain why it is triple ported. **10**
   (b) Explain how are interrupts routed in PCI bus? Give suitable example. Also explain use of Interrupt Pin register and Interrupt Line register. **10**

2. (a) Explain instruction paring rules in Pentium processor. **10**
   (b) Explain how coherency is maintained between L1 data cache of Pentium Processor, L2 cache and main memory. **10**

3. (a) Explain with a neat diagram data bus steering while executing 32 bit data read instruction. Assume 16 bit device interfaced to Pentium processor.
   Indicate how many bus cycles are run for this operation. **12**
   (b) Explain following signals in Pentium Processor INIT, LOCK#, SCYC, R/S# **8**

4. (a) Explain with neat diagram protocol for PIO read command in IDE. **10**
   (b) Explain the difference between synchronous and asynchronous data phase in SCSI. **10**

5. (a) Explain the process of Device Enumeration in USB devices. **10**
   (b) Explain Following signals in SCSI **10**
   ATN, MSG, BSY, REQ, ACK

6. (a) Master A wants to perform 2 transactions as 2 data writes from device C, **12**
   2 data reads from device D
   Master B wants to perform 3 data reads from device D
   Master A & B request together, and priority of master B is less than that of A.
   Explain transactions performed with timing diagrams.
   (b) Explain bus parking in PCI bus. **8**

7. (a) Explain Reflected wave switching used in PCI bus. **5**
   (b) Explain the use of Branch Target Buffer in Pentium processor. **5**
   (c) Explain methods of invalidating cache lines for Pentium processor. **5**
   (d) Explain different data transfer types in USB. **5**

BE sem VII. Filter Design

ETRX

21/11/2014

QP Code : 15285

(3 Hours) **[Total Marks : 100**

N.B.: (1) Question No. 1 is **compulsory**.
(2) Attempt any **four** from remaining questions.
(3) **Figures** to the **right** indicate **full** marks.
(4) Assume **suitable** data if **necessary**.

1. Attempt any **four** from following :– **20**
   (a) State the concept of adaptive filter
   (b) Explain quadrature mirror filtering in multirate DSP
   (c) Write a short note on prewarping.
   (d) Explain the principle of switched capacitor filter
   (e) Compare FIR and IIR filter

2. (a) Explain Gibb's phenomenon. State its significance in FIR filter design. **10**
   (b) What is FDNR? State its properties. Explain synthesis of low pass functions using FDNR. **10**

3. (a) Apply bilinear transformation to convert $H(s) = \frac{2}{(s+1)(s+2)}$ to H(z) with T=1 sec. **10**
   (b) Explain the effect of decimation and interpolation in time and frequency domain. **10**

4. (a) Design analog chebyshev filter with maximum passband attenuation of 3 dB at $\Omega p = 200$ rad/sec and stopband attenuation of 60 dB at $\Omega s = 1500$ rad/sec. **10**
   (b) Design low pass FIR linear phase filter with 11 coefficients by using Hamming window for following specifications : **10**
   Passband frequency: 0.25 KHz
   Sampling frequency: 1 KHz

5. (a) Explain leap frog realization technique with suitable example. **10**
   (b) State working principle of Weiner filter. **5**
   (c) Explain the concept of subband coding. **5**

[TURN OVER

6. (a) Design digital FIR filter with 10

$$H_d(e^{jw}) = e^{-j3w} \text{ for } -\frac{\pi}{4} \le |w| \le \frac{\pi}{4}$$

$$= 0 \qquad \text{for } \frac{\pi}{4} \le w \le \pi$$

Use Blackman window with N = 7.

(b) Determine the order and poles of Lowpass Butterworth filter that has a 3 dB attenuation at 500 Hz and attenuation of 40 dB at 1000 Hz. 10

7. Write short notes on :– 20

(a) Why antialising /antiimaging required

(b) What is inductance simulation ? Explain

(c) MMSE criteria in adaptive filters

(d) Matched Z transform

B.E. ETRX Sem VII (R)&(Old). 9/12/14.

VLSI Design

QP Code :15487

(3 Hours) **Total Marks : 100**

N. B. : (1) Question **No. 1** is **compulsory.**
(2) Attempt any **four** questions from remaining **six** questions.
(3) Assume **suitable** data wherever **necessary.**
(4) Figures to the right **indicate** marks.

1. (a) Draw a energy band diagram of MOS capacitor under external bias. **5**
(b) Compare buried and butting contact **5**
(c) Implement following function using CMOS. **5**
$F = \overline{a.b + c.d + e}$
(d) Draw the stick diagram for CMOS NOR gate. **5**

2. (a) Explain the various parameter affecting the threshold voltage of MOSFET. Explain the effect of ion implantation on threshold voltage of MOSFET. **10**
(b) Explain the complete fabrication process steps for CMOS inverter using n-well process with the help of cross sectional diagram with all masking steps. **10**

3. (a) A CMOS symmetric inverter has following parameter **10**
$V_{DD} = 3.3V$, $V_{tn} = 0.6V$, $V_{tp} = -0.7v$.
$k_n = 200\ \mu A/V^2$ $k_p = 80\ \mu A/V^2$
Calculate noise margin of the circuit.
(b) Define scaling.Discuss the advantages and disadvantages of different types of scaling. **10**

4. (a) Draw circuit diagram, stick diagram and layout for two input NOR gate using CMOS design rules. **10**
(b) Explain the operation of CMOS inverter with clearly mentioning the five cases given below. **10**
(i) $V_{in} < V_{tn}$ (ii) $V_{in} = V_{IL}$
(iii) $V_{in} = V_{IH}$ (iv) $V_{in} > V_{DD} + V_{tp}$
(v) $V_{in} = V_{TH}$ (Inverter threshold)

5. (a) Write a verilog code for 4 bit ripple counter using D-FF as a basic component **10**
(b) Compare passive load, active load NMOS inverter circuit with advantages and disadvantages. **10**

6. (a) Implement following boolean function using CMOS logic **10**
$y = \overline{x.y.z + x.w.y}$
Draw stick diagram and layout of the circuit.
(b) What is latch up in CMOS inverter and how to avoid it. **10**

7. Write short notes on **any three**:– **20**
(a) Hot electron effect
(b) Y-chart for design flow
(c) Design rules and their necessity
(d) Oxidation

LM-Con.:10475-14.

BE. SEM VII (Rev) - CN (E1R+) 15 Dec 2014

QP Code :156

(3 Hours) **[Total Marks : 100**

N.B. : (1) Question No.**1** is **compulsory**.
(2) Answer any **four** out of the remaining **six** questions.
(3) Illustrate answers with **sketches** wherever **required**.

1. Answer any **four** of the following :— **20**
   (a) Compare the performance characteristics of co-axial, twisted pair and fiber optic transmission media.
   (b) Explain various LAN topologies.
   (c) What is meant by 'blocking' in switched networks ? Bring out the merits and demerits of a single stage space division switch.
   (d) Explain general principles of congestion control in Packet switching networks.
   (e) Explain Berkley API.

2. (a) Compare circuit switching, packet switching and message switching. **10**
   (b) What is Flow control ? Explain Sliding window flow control with neat diagrams. How is the window size Determined ? **10**

3. (a) Explain in detail O.S.I. model. **10**
   (b) What is DSL technology ? Explain various DSL technologies and compare them. **10**

4. (a) Draw the block diagram of SO NET and explain its operation. Also explain SONET frames. Explain the functional layers of SO NET. **10**
   (b) With reference to HDLC, Explain the following :— **10**
      (i) various frames of HDLC.
      (ii) Data transfer modes.
      (iii) Data transparency.
      (iv) Unbalanced and balanced configuration.
      (v) Piggy backing and Pipelining.

5. (a) Explain the different ARQ techniques in detail and state which ARQ technique is preferred for noisy links ? And why ? **8**
   (b) Design a three stage Space division switch with N = 15, n = 5, K = 3 and show how Blocking occurs in this. Derive the condition required to make this switch non-Blocking. **6**
   (c) Discuss various Routing strategies for packet switching networks. **6**

6. (a) Explain the following network connecting devices :— 10
(i) switches (ii) routers (iii) gateway (iv) hub (v) bridge.

(b) Explain the MAC sublayer Frame format for IEEE802 Reference ? Explain Fast Ethernet specifications. Also explain CSMA-CD in detail. 10

7. Write short notes on :— 20
(a) ISDN.
(b) Sub-netting and Super-netting with an example.
(c) IP utilities.
(d) Token Re-insertion Strategies.

———v———