EXTC OLD sem III AM-III
EXSTC OTR

Q.P. Code : 544201

(3 hours) **Marks : 100**

Note : 1) Question no. **ONE** is **compulsory.**
2) Attempt any **FOUR** questions out of the remaining six questions.
3) Figures to right indicate full marks.

1. a) Find Laplace transform of sint sin2t sin3t **5**
   b) Find z- transform of $\{a^{|k|}\}$ **5**
   c) Obtain complex form of Fourier series for $f(x) = \sinh(ax)$ in $(-l, l)$ **5**
   d) Show that every square matrix can be uniquely expressed as the sum of a Hermitian and skew- Hermitian matrix. **5**

2. a) Find Laplace transform of $\left(\int_0^t e^{-4u}\sin^2(u)du\right)$ **6**
   b) If $A = \begin{bmatrix} 0 & 2m & n \\ l & m & -n \\ l & -m & n \end{bmatrix}$ is orthogonal ,find l, m, n. Also find A^{-1} . **6**
   c) Find the Fourier expansion for $f(x) = \sqrt{1-\cos(x}$ in $(0, 2\pi)$ **8**

3. a) Test for consistency and solve **6**
   $2x - 3y + 5z = 1,\ 3x + y - z = 2,\ x + 4y - 6z = 1$
   b) Find the Fourier expansion for $f(z) = 9 - x^2$ in $(-3, 3)$ **6**
   c) Find inverse z-transform of $f(x) = \dfrac{3z^2 - 18z + 26}{(z-2)(z-3)(z-4)}, \quad 3 < z < 4$ **8**

4. a) Solve Using Laplace transform dt $\dfrac{d^2y}{dt^2} + y = t$ where $y'(0) = 0, y(0) = 1$ **6**
   b) Find the Fourier expansion for $f(x) = 2x - x^2$ in $(0, 3)$ **6**
   c) Find z- transform of $c^k \sinh(\alpha k), \quad k \geq 0$ **8**

[TURN OVER]

5. a) Find fourier integral representation for $f(x) = \begin{cases} 1-x^2 & \text{for } |x| \le 1 \\ 0 & \text{for } |x| > 1 \end{cases}$ 6

b) Find the two non -singular matrices P and Q such that 6

PAQ is in nomml form where $A = \begin{bmatrix} 1 & 1 & 0 \\ 1 & 2 & -1 \\ 2 & 3 & 1 \end{bmatrix}$ and also. find its rank

c) Obtain fourier series for $f(x) = 2x - x^2$, $0 < x < 2$ as a half range cosine series and sine series. 8

6. a) Using Laplace transform evaluate 6

$\int_0^\infty e^{-t}(1+2t-t^2+t^3)H(t-1)dt$

b) Find inverse Laplace transform of $\tan^{-1}\left(\frac{2}{s^2}\right)$ 6

c) Find inverse Laplace transform of the following 8

(i) $\frac{1}{s}\tan^{-1}\left(\frac{a}{s}\right)$ (ii) $\frac{(s+1)e^{-s}}{s^2+2s+2}$

7. a) Find inverse Laplace transform of $\frac{1}{(s^2+4s+13)^2}$ by convolution theorem 6

b) Show that the matrix $A = \frac{1}{2}\begin{bmatrix} \sqrt{2} & -t\sqrt{2} & 0 \\ i\sqrt{2} & -\sqrt{2} & 0 \\ 0 & 0 & 2 \end{bmatrix}$ is a unitary matrix and 6

Hence find A^{-1} 8

c) Obtain fourier series for $f(x) = x\sin(x)$ in $(-\pi, \pi)$

Hence deduce that $\frac{\pi-2}{4} = \frac{1}{1.3} + \frac{1}{3.5} + \frac{1}{5.7} + \text{---}$

Sem III Extc (old) EDC – I 2/12/16

Q.P. Code : 544300

(3 Hours) **[Total Marks : 100**

N.B. : (1) Question **No.1** and **No.2** are **compulsory**.
(2) Answer **any three** questions from remaining questions.
(3) **Figures** to the **right** indicate **full marks**.
(4) Assume suitable **data** if **required**.

1. Design single stage RC coupled C E amplifier for following specifications : **20**
$A_V \geq 160$, $V_{CEQ} = 6.5V$, $I_{CQ} = 2.5mA$, $F_L = 20$ Hz. Use $V_{CC} = 15V$. Determine voltage gain, input impedance, output impedance.

2. Design single stage CS amplifier employing JFET type BFW11 for the following specifications : $A_V \geq 15$, $I_{DQ} = \frac{I_{DSS}}{5} mA$, $V_{CC} = 21V$ and $F_L = 20Hz$. **20**
Determine voltage gain, input impedance, output impedance.

3. (a) Design fixed bias circuit with emitter resistance for $I_{CQ} = 1.2mA$, $V_{CE} = 5V$, $V_E = 1.5V$ and $\beta = 60$. Assume $V_{CC} = 9V$. Also derive the expression for stability factor for the above bias circuit. **10**
(b) Draw small signal hybrid parameter equivalent circuit for CB amplifier and define the same. What are the advantages of *h*-parameters? **10**

4. (a) For the amplifier shown in figure.1 analyze and determine : **10**
(i) I_{CQ}, V_{CEQ}, V_C, V_E
(ii) Small-signal voltage gain
(iii) Input and output impedance
The circuit parameters are :
$R_1 = 56k\Omega$, $R_2 = 12.2k\Omega$, $R_E = 0.4k\Omega$, $R_C = 2k\Omega$, $R_L = 10k\Omega$, $R_S = 0.5k$, $V_{CC} = 10V$ and BJT parameters are $\beta = 100$, $V_{BE} = 0.7V$.

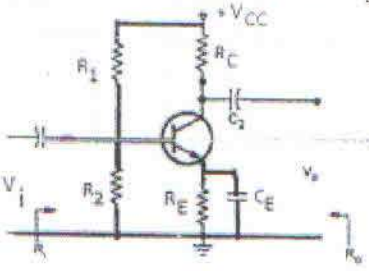

Fig. 1

TURN OVER

(b) Draw circuit diagram of JFET small signal Common Source amplifier (with any biasing) and derive the expression for, small signal mid-band voltage gain, input impedance and output impedance. **10**

5. (a) Explain the biasing techniques for D-MOSFET and E-MOSFET. **10**

(b) Design voltage divider biasing JFET for the following parameters : **10**

$I_{DSS} = 4mA$, $V_P = -2V$

The circuit parameters :

$R_D = 1k\Omega$, $R_1 = 12M\Omega$, $I_{DQ} = 3.4mA$, and $V_{DS} = 10.5V$, $V_{DD} = 21V$.

6. (a) What is bleeder resistance? **10**

Design L section LC filter with full wave rectifier to meet following specifications : The DC output voltage $V_{DC} = 200V$, deliver $I_L = 50mA \pm 20mA$ to the resistive load, and required ripple factor is 0.04.

(b) Design a simple Zener voltage regulator to meet the following specifications: **10**

Output voltage $V_0 = 6.2V$, Load current $I_{Lmax} = 50mA$, $I_{Lmin} = 0.1mA$, $I_{zmax} = 90mA$, $I_{zmin} = 5mA$, $P_Z = 420mW$ and Input voltage $V_i = 20V$ to 30V.

7. Write short notes on following (**any two**) : **20**

(a) Construction and Characteristics of SCR

(b) Diode compensation for I_{CO} techniques

(c) Construction and Characteristics of E-MOSFET

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Transistor type	P_{dmax} @ 25°C Watts	I_{cmax} @ 25°C Amps	V_{CE} (sat) volts d.c.	V_{CBO} volts d.c.	V_{CEO} (Sus) volts d.c.	V_{CEX} (Sus) volts d.c.	V_{EBO} volts d.c.	T_j max °C	D.C. current gain min	typ.	max.	Small Signal h_{fe} min.	typ.	max.	V_{BE} max.	θ_{ja} °C/W	Derate above 25°C W/°C
2N 3055	115·5	15·0	1·1	100	60	70	90	7	200	20	50	70	15	50	120	1·8	1·5	0·7
ECN 055	50·0	5·0	1·0	60	30	55	60	5	200	25	50	100	25	75	125	1·5	3·5	0·4
ECN 149	30·0	4·0	1·0	50	40	—	—	8	150	30	50	110	33	60	115	1·2	4·0	0·3
ECN 100	5·0	0·7	0·6	70	60	65	—	6	200	50	90	280	50	90	280	0·9	35	0·05
BC147A	0·25	0·1	0·25	50	45	50	—	6	125	115	180	220	125	220	260	0·9	—	—
2N 525(PNP)	0·225	0·5	0·25	85	30	—	—	—	100	35	—	65	—	45	—	—	—	—
BC147B	0·25	0·1	0·25	50	45	50	—	6	125	200	290	450	240	330	500	0·9	—	—

Transistor type	h_{ie}	h_{oe}	h_{re}	θ_{ja}
BC 147A	2·7 K Ω	18μ ℧	$1·5 \times 10^{-4}$	0·4°C/mw
2N 525 (PNP)	1·4 K Ω	25μ ℧	$3·2 \times 10^{-4}$	—
BC 147B	4·5 K Ω	30μ ℧	2×10^{-4}	0·4°C/mw
ECN 100	500 Ω	—	—	—
ECN 149	250 Ω	—	—	—
ECN 055	100 Ω	—	—	—
2N 3055	25 Ω	—	—	—

BFW 11—JFET MUTUAL CHARACTERISTICS

$-V_{GS}$ volts	0·0	0·2	0·4	0·6	0·8	1·0	1·2	1·6	2·0	2·4	2·5	3·0	3·5	4·0
I_{DS} max. mA	10	9·0	8·3	7·6	6·8	6·1	5·4	4·2	3·1	2·2	2·0	1·3	0·5	0·0
I_{DS} typ. mA	7·0	6·0	5·4	4·6	4·0	3·3	2·7	1·7	0·8	0·2	0·0	0·0	0·0	0·0
I_{DS} min. mA	4·0	2·5	2·2	1·6	1·0	0·5	0·0	0·0	0·0	0·0	0·0	0·0	0·0	0·0

N-Channel JFET

Type	V_{DS} max. Volts	V_{DG} max. Volts	V_{GS} max. Volts	P_d max. @25°C	T_j max.	I_{DSS}	g_{os} (typical)	$-V_p$ Volts	r_d	Derate above 25°C	θ_{ja}
2N3822	50	50	50	300 mW	175°C	2 mA	3000 μ ℧	6	50 KΩ	2 mW/°C	0·59°C/mW
BFW 11 (typical)	30	30	30	300 mW	200°C	7 mA	5600 μ ℧	2·5	50 KΩ	—	0·59° C/mW

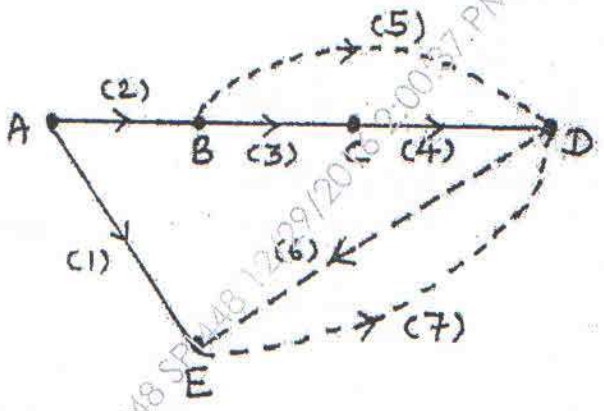
SEM-III EXTC (old) 29/12/16 **Q.P. Code : 544601**

Electrical Networks **(3 Hours)** **[Total Marks : 100]**

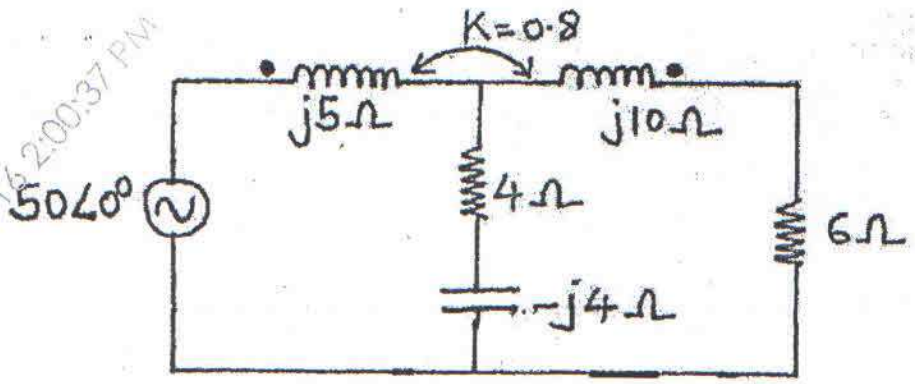
NB: 1) Question No.**1** is **compulsory**.
2) Attempt any **four** from the **remaining** questions.
3) **Assume** suitable **data**, if **required**.

1. (a) Find the condition of reciprocity for Z parameters. **05**
(b) Write short note on interconnections of two port networks. **05**
(c) Draw Laplace equivalent circuits for R, Land C taking into account initial conditions. **05**
(d) Test whether following polynomials are Hurwitz or not. **05**
i) s^2+8 ii) $(s+2)^3$

2. (a) Linear graph of a network is shown below. For the given tree (shown with firm lines) **10** obtain-
(i) Fundamental cutset matrix
(ii) Fundamental tieset matrix.

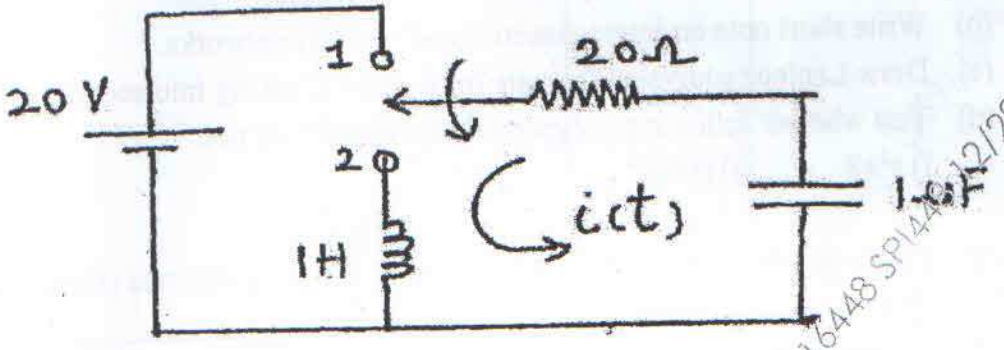


(b) Find the voltage across 6 Ω resistor using mesh analysis. **10**



TURN OVER

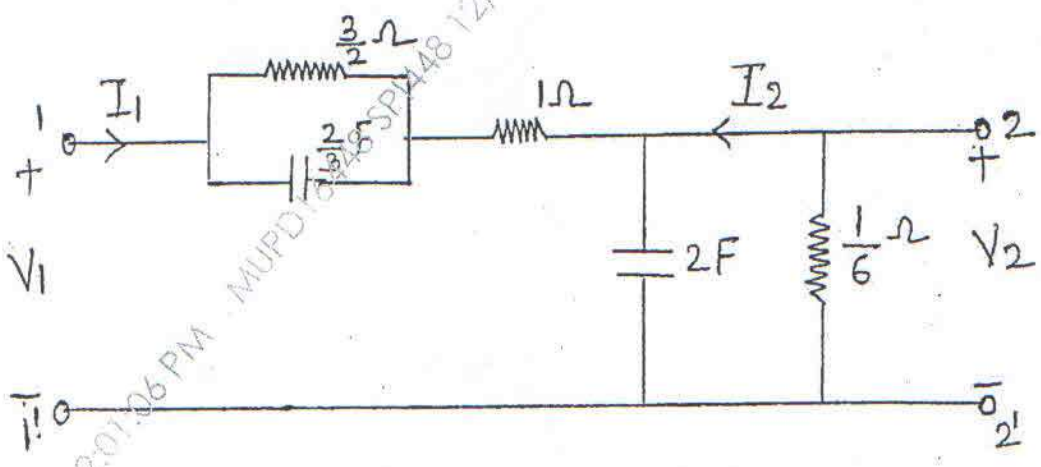
3. (a) For the given the given network, the switch is changed from position 1 to 2 at time t=0. Find i, $\frac{di}{di}$ and $\frac{d^2i}{dt^2}$ at t=0+. Assume that steady state condition is reached at switch position 1. **10**



(b) Realize following impedance function using Foster-II and Foster-II form. **10**

$$Z(s) = \frac{4(s^2+1)(s^2+9)}{s(s^2+4)}$$

4. (a) For the given network, find out $\frac{V_1}{I_1}, \frac{V_2}{V_1}$ **10**



(b) Check the positive realness of the following functions: **10**

$$\text{(i) } F(s) = \frac{(s+3)}{(s+1)} \quad \text{(ii) } F(s) = \frac{s(s+3)(s+5)}{(s+1)(s+4)}$$

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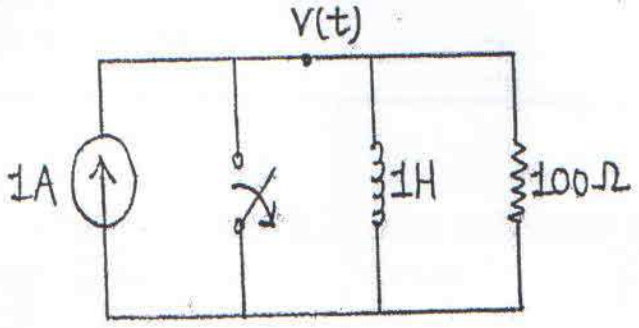
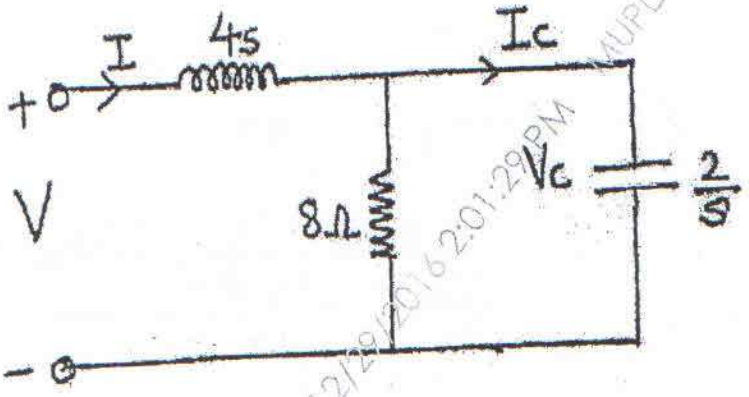
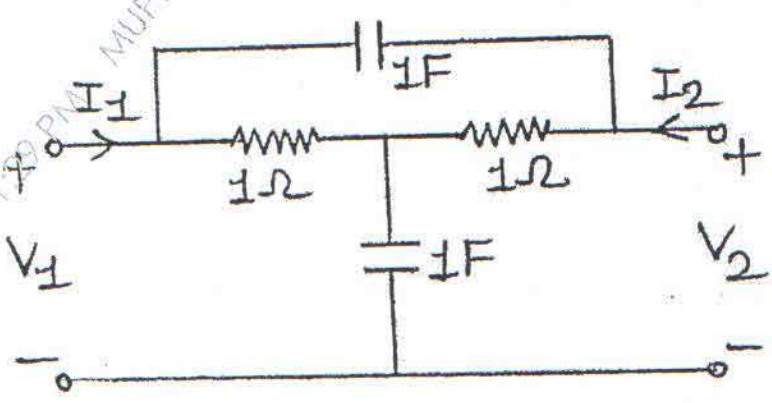
5. (a) For the given network at t = 0, switch is opened. Calculate v, $\frac{dv}{dt}$, $\frac{d^2v}{dt^2}$ at $t=0^+$. 10



5. (b) For the network shown below find $\frac{Vc}{V}$. 10



6. (a) Find y parameters for the given network. 10



(b) Analyze series RL circuit in time domain and explain natural and forced response. 10

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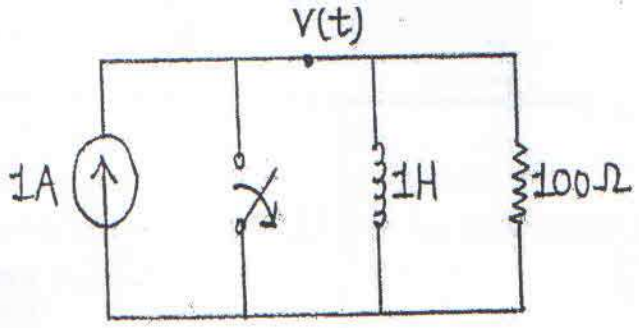
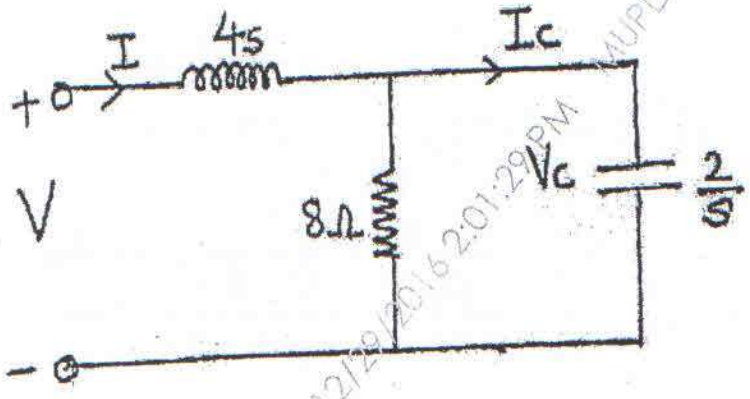
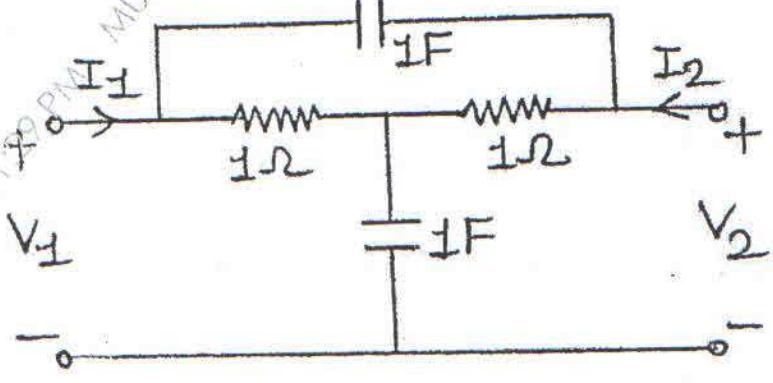
5. (a) For the given network at t = 0, switch is opened. Calculate v, $\frac{dv}{dt}$, $\frac{d^2v}{dt^2}$ at $t=0^+$. 10



5. (b) For the network shown below find $\frac{V_c}{V}$. 10



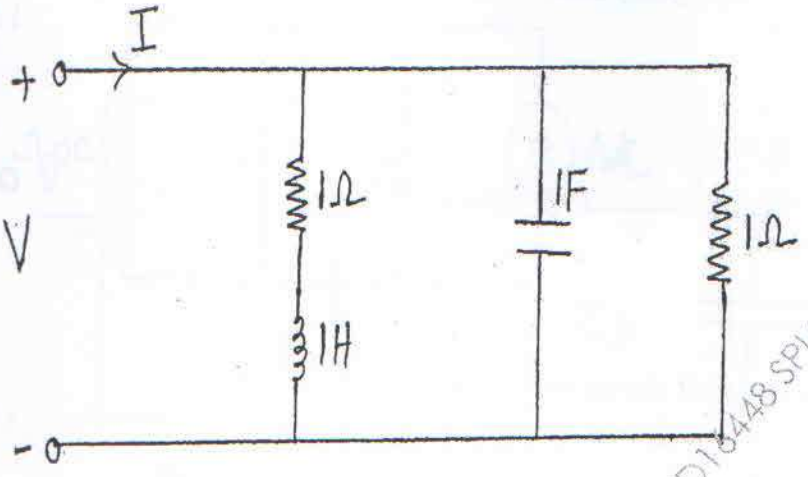
6. (a) Find y parameters for the given network. 10



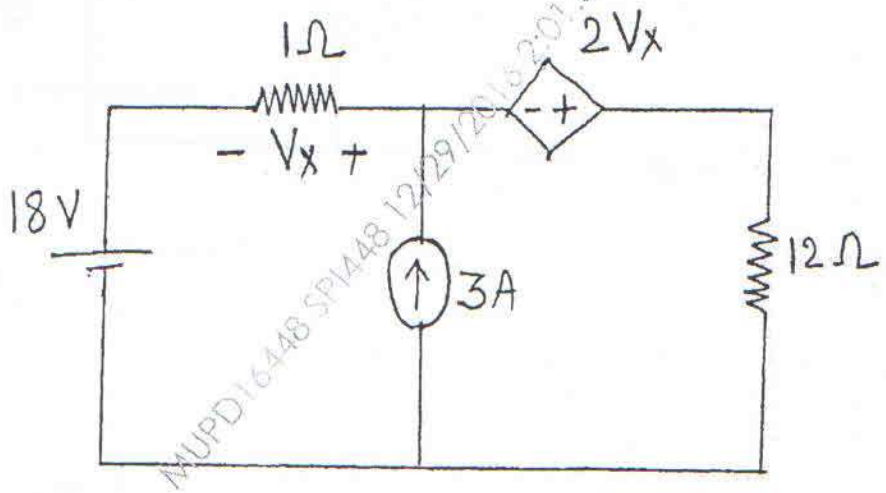
(b) Analyze series RL circuit in time domain and explain natural and forced response. 10

TURN OVER

7. (a) Find the driving point Y(s) for the network shown below and plot the pole zero diagram. **10**



(b) Find the current through 12 Ω resistor using Norton's theorem. **10**



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Sem III (old) EXTC 09/12/16

Digital Logic Design **QP Code : 544401**

(3 Hours) **[Total Marks : 100**

N.B. : (1) Question **No. 1** is **compulsory.**
(2) Solve any **four** questions out of remaining **six.**
(3) Each question carries **20** Marks. Equal marks for the subquestions.
(4) Assume suitable data if required.

1. (a) Explain Minterm and Maxterm
   (b) Explain set, Reset, Preset and clear related to Flip-flops.
   (c) Explain various characteristics of logic families.
   (d) Explain various Binary codes with examples.

2. (a) State and Prove DeMorgan's theorems.
   (b) Design Full Adder using Logic gates.

3. (a) Minimize the following logical function using K-map.
   $f(A,B,C,D) = \pi M (4,5,6,7,8,12). d (1,2,3,9,11,14)$
   (b) Design 3 bit binary up Ripple counter using MS-JK Flip Flops and explain its working with output waveforms.

4. (a) Explain TTL Logic family.
   (b) Minimize the following logical function using Quine-McCluskey method.
   $f(A,B,C,D) = \Sigma_m (0,1,3,7,8,9,11,15)$

5. (a) (i) Design Y= A+BC using NAND gates only.
   (ii) Convert D-Flip-flop into T- FlipFlop.
   (b) Design 3-bit Binary code to Gray code converter using a Decoder with few gates.

6. (a) Design 16:1 Multiplexer using all 4:1 Multiplexers.
   (b) With neat sketch draw and explain the working of 3-bit SISO Register with output waveforms.

7. Write short notes on any **four** of the following :-
   (i) CMOS Logic family
   (ii) FPGA
   (iii) Number systems
   (iv) Asynchronous counter
   (v) PAL and PLA
