

(REVISED COURSE)

(3 Hours)

[Total Marks : 100]

- N.B. :**
- (1) Question No. 1 is compulsory.
 - (2) Answer any four out of remaining six questions.
 - (3) Assumptions made suitable clearly stated.
 - (4) Assume suitable data wherever required but justify the same.
 - (5) Figures to the right indicate full marks.
 - (6) Illustrate answers with sketch wherever required.
 - (7) Answers to questions should be grouped and written together i.e. all answers to subquestions of individual questions like Question No. 1, 2, 3 etc. should be answered one below the other.
 - (8) Use legible handwriting. Use blue/black ink pen to write answers. Use of pencil should be done only to draw diagrams and graph.

1. (a) How might you use a field transistor to prevent over voltage in a CMOS chip ? 4
- (b) A pad requires a pull up resistor, which is implemented as a p-transistor that has the source connected to V_{ss}. Does this structure require any latchup protection ? What about on n pulldown ? 4
- (c) Consider in IC npn transistor Q₁ built upon a p type substrate S. Show that between the 4 terminals E, B, C and S there exist a p-n-p transistor Q₂ in addition to Q₁. If Q₁ is in its active region, in what mode is Q₂ operating ? Explain. 4
- (d) Sketch the five basic diode connections for the monolithic integrated circuits. Which will have the lowest forward voltage drop ? Highest breakdown voltage ? 4
- (e) Explain why different criteria might be used to size transistor in lightly coupled small fanout circuit versus widely spaced high fanout circuits. 4
2. (a) Explain how to estimate multiple conductor routing capacitances. 10
- (b) List in order the steps required in fabricating a monolithic silicon integrated transistor by the epitaxial diffused method. Sketch the cross section after each oxide growth. Label materials clearly. No buried layer is required. 10
3. (a) What is the minimum number of isolation regions required to realize in monolithic form for 2 input TTL NAND gate. Draw monolithic layout of this gate. 10
- (b) Draw the stick diagram and a mask layout for an 8 i/p NMOS inverter circuit. Both the input and output points should be on the polysilicon layer. 10
4. (a) Explain the limits of interconnect, logic levels and supply voltage of MOS circuits. 10
- (b) A particular layer of MOS circuit has a resistivity $\rho = 1 \text{ ohm-cm}$. A section of this layer is $55 \mu\text{m}$ and $5 \mu\text{m}$ wide and has a thickness of $1 \mu\text{m}$. Calculate the resistance from one end of this section to the other. Use the concept of sheet resistance RS. What is the value of RS ? 10
5. (a) An off chip capacitance load of 5 PF is to be driven from NMOS invertors. Set out suitable arrangements giving appropriate channel L:W ratios and dimensions. Calculate the number of inverter stages required and the delay exhibited by the overall arrangement driving the 5 PF load. 10
- (b) Using the λ design rules, sketch a simple layout of CMOS inverter on graph paper. Use a minimum feature size of $3 \mu\text{m}$. Neglect the substrate connection. 10
6. (a) Describe float zone single crystal growth process. 10
- (b) What are the major problems associated with a single threshold voltage adjust implant ? 5
- (c) What are the major trade offs in using a wet process or a dry process when growing thermal SiO₂ ? 5
7. (a) Estimate the delay through a $250 \text{ k}\Omega$ resistors made using an n-well with a width of $3 \mu\text{m}$ and a length of $300 \mu\text{m}$. 6
- (b) A CMOS process produces gate oxides with a thickness of $t_{ox} = 100 \text{ \AA}$. The FET carrier mobility values are given as $\mu_n = 500 \text{ cm}^2/\text{V-sec}$ and $\mu_p = 210 \text{ cm}^2/\text{V-sec}$. Calculate the oxide capacitance per unit area in units of $\delta F/\mu\text{m}^2$. Find the process transconductance values for nFETS and PFETS. 10
- (c) Discuss briefly the relationships between an ion beam's acceleration potential, the beam current and the time of implantation on the resulting doping profile. 4