

OCTOBER 2006

Logic Design

[ REVISED COURSE ]

CON/4948-06.

YM-5278

25/6/06

( 3 Hours )

[ Total Marks : 100

- N.B.:**
- 1) Question No. I is Compulsory.
  - 2) Attempt any four out of the remaining Six.
  - 3) Figures to the right indicate full marks.
  - 4) Draw logic circuit diagram to illustrate your answer.
  - 5) Assume suitable data if required.
- I**
- A) Using Two's Complement Method subtract  $(47)_8$  from  $(47)_{10}$ . 20
  - B) Design X-OR and X-NOR gates using all the universal gates.
  - C) With the neat logical internal circuit diagram, explain the 8L : 1L Multiplexer.
  - D) State the different Laws of Boolean Algebra.
- II**
- A) With reference to Preset, Clear, Clock, Set and Reset, explain SR flip flop along with the internal circuit diagram using NAND gates only. 10
  - B) Implement the following function using all 4L : 1L Multiplexer 10
    1.  $F(ABC) = \pi(0, 1, 4, 5, 7)$ .
    2.  $F(PQRS) = \Sigma(1, 2, 6, 7, 9, 11, 13, 15)$ .
- III**
- A) Design and implement a BCD to 7 Segment Decoder for common cathode configuration. 20
- IV**
- A) Draw and explain Bidirectional Shift Register. 10
  - B) Explain BCD Subtraction using 4- Bit Adder with an example. 10
- V**
- A) Design Synchronous Decade Counter 10
  - B) Simplify the following equations 10
    1.  $A.B + \overline{A}.C = AB + \overline{B.C} + A.C$
    2.  $\overline{[ABC + \overline{A} \overline{B}] + AC}$
- VI**
- A) Design Full Adder and Full Subtractor. 10
  - B) Design the sequential circuit for the following sequence (0-3-6-4-5-1-2-7-0). 10
- VII**
- Write short notes on any two: 20
- 1) Comparisons between TTL, CMOS, ECL Logic Families.
  - 2) PAL and PLA.
  - 3) Combinational and Sequential circuits.
  - 4) Encoder and Decoder.