

S.E Comp I T.

C. O. A

23/5766

Con. 2846-06.

(REVISED COURSE)  
( 3 Hours)

TV - 8124

[Total Marks : 100

P320UP000E-4-28 166

N. B. : (1) Question No. 1 is **compulsory**.

(2) Attempt any **four** from **remaining** questions.

1. (a) Consider the unpipelined machine with 10 ns clock cycles. It uses 4 cycles for ALU operations and branches whereas 5 cycles for memory operations. Assume that the relative frequencies of these operations are 40%, 20% and 40% respectively. Suppose that due to clock skew and setup, pipelining the machine adds 1 ns overhead to the clock. How much speed up in the instruction execution rate will we gain from a pipeline ? 10  
(b) Explain TLB. 10
2. (a) Suppose a cache is 10 times faster than main memory and suppose that the cache can be used 90% of the time. How much speed up do we gain by using the cache. 10  
(b) Explain disk performance parameters. 10
3. Design and implement Booth's multiplier circuit using hardwired (use delay element method and sequence counter method) and microprogrammed (use Wilkies design) control unit design methods. 20
4. (a) Explain interrupt driven I/O. 10  
(b) Explain the impact of page size and segment size on space utilization. Draw graph for space utilization versus segment size by taking page size 512 and 1024. 10
5. (a) Explain Flynn's classification. 10  
(b) Explain restoring division method. Hence perform  $-7 \div -3$ . 10
6. (a) Explain fetch cycle, indirect cycle and interrupt cycle. 10  
(b) Write and explain the microprogram for ADD R1, (R3). 10
7. Write short notes :— 20
  - (a) Synchronous DRAM
  - (b) Floating point ALU
  - (c) PCI bus
  - (d) DMA.