S.E Etrx IV D. D – II 10/6/06

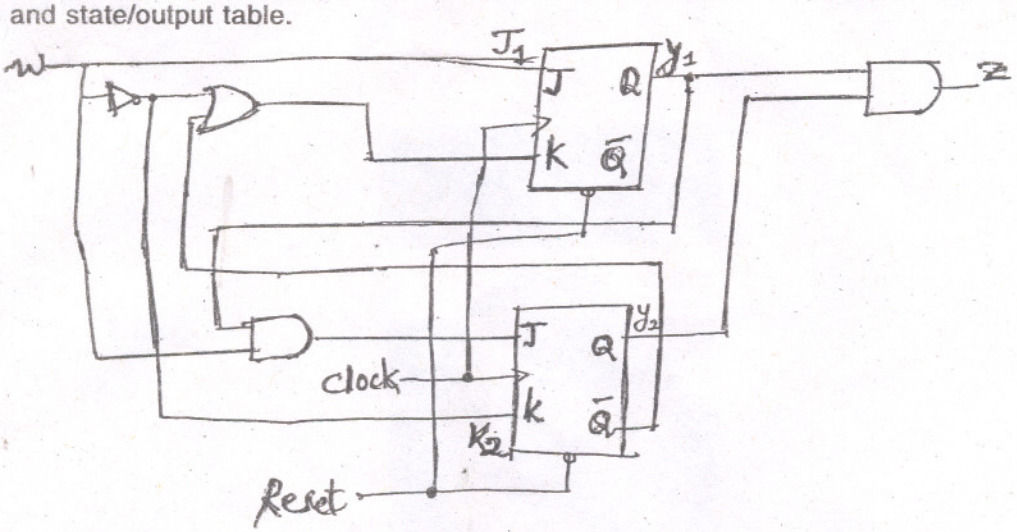
P May 06, 3 269

Con. 1899-06. (REVISED COURSE) TV-8118

(3 Hours) [Total Marks : 100

N.B. (1) Question No. **1** is **compulsory**.
(2) Attempt any **four** out of remaining **six** questions.

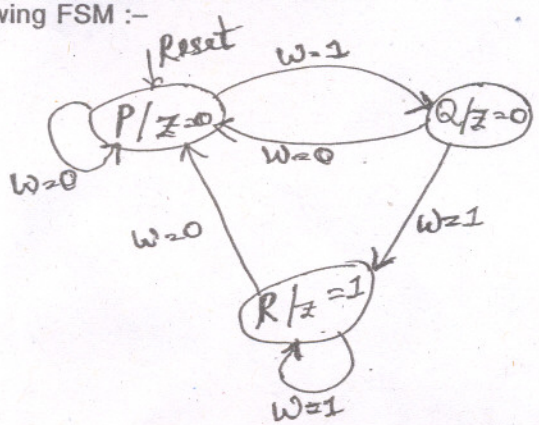
1. (a) Analyze the clocked synchronous machine given below. Write excitation equations, excitation/transition tables and state/output table. **10**



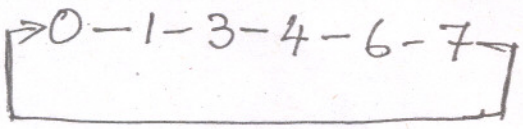
(b) Design a MOD-100 counter using IC 7493. **10**

2. (a) Design a coin operated vending machine that dispenses chocolates under the following condition :– **12**
(i) The machine accept Re. 1 and Rs. 2 as coins.
(ii) It takes Rs. for a chocolate to be released from machine.
(iii) If Rs. 4 is deposited, the machine will credit the buyer with Re. 1 and wait for the buyer to make a second purchase.
Follow all the steps including state decomposition and state assignment in designing a MOORE machine.
(b) Draw a switch debouncer using NAND gates and explain. **8**

3. (a) Draw and Explain the logic diagram for 8 × 4 diode ROM. **10**
(b) Write the VHDL code for the following FSM :– **10**



4. (a) Design a asynchronous counter using JK flip-flops which goes through a sequence of :– **10**



Flipflop responds to the negative edge of a clock pulse. The counter should reset to zero state whenever it encounters an unused state.
(b) Draw the universal state diagram for a 4 bit serial in parallel out right shift register. Using it to design a twisted ring counter. **10**

5. (a) Write a VHDL program for a 8 bit bidirectional shift register. **10**
(b) Examine the working of a SRAM cell. Also show how an array of the cells form a SRAM block and so a memory unit. **10**

6. (a) Give the main features of Xilinx XC 9500 CPLD family. **10**
   (b) Discuss the main issues related to the estimation of Digital System Reliability. **10**

7. Write notes on (any **two**) :– **20**
   (a) CAD Tools
   (b) VHDL
   (c) XC 4000 FPGA family.
