

(3 Hours)

[Total Marks : 100

- I.B. : (1) Question No.1 is compulsory.
 (2) Attempt any four of the remaining six questions.
 (3) Assume suitable data wherever necessary.
1. (a) What are the different ways to adjust the threshold voltage of a MOS transistor. 5
 (b) When is a MOS transistor called a short channel device. Give reasons. 5
 (c) Give the merits and demerits of ion implantation and diffusion process. 5
 (d) With the help of a neat diagram explain the important features of butting and buried contacts. 5
2. (a) Consider a PFET that has a gate oxide thickness of $t_{ox} = 60 \text{ \AA}$, the hole mobility $\mu_p = 220 \text{ sq.cm/v-sec}$, aspect ratio $W/L = 12/1$. Assume $V_{DD} = 3.3 \text{ V}$, $V_{tp} = -0.7 \text{ V}$
 (i) Calculate the process transconductance of the FET.
 (ii) Find the device transconductance and resistance.
 (b) Discuss the parasitic effects in MOSFETS. 10
3. (a) Compare the two technologies of scaling methods – 10
 (i) constant electric field scaling
 (ii) constant power supply voltage scaling
 Also show how delaytime, power dissipation and power density is affected in terms of scaling factor α .
 (b) A silicon MOS system with p type substrate, $N_a = 10^{15} / \text{c.c}$, $\epsilon_{r,ox} = 3.9$ and oxide thickness of 100 \AA is at the onset of strong inversion. Determine;
 (i) width of the depletion layer.
 (ii) The charge density in the depletion layer.
 (iii) The electron density n_s at the surface
 (iv) The threshold voltage
 Given $\epsilon_r(\text{Si}) = 11.8$, $n_i(\text{Si}) = 1.5 \times 10^{10} / \text{c.c}$
4. (a) With neat diagrams explain the fabrication sequence of CMOS inverter using the n-well process. 10
 (b) What is epitaxy? What are the different epitaxial processes? Explain one of them in detail. 10
5. Use the CMOS design rules to design a 2 input NAND gate with an inverter ratio of 4 and depletion mode pullup device. Include V_{dd} and ground bus lines. Use the buried contact and take the output on polysilicon. Show the connection for substrate and well also. Draw the circuit diagram, stick diagram and mask layout, to scale 20
6. (a) What is photolithography? What are the different techniques involved in it. Explain one of them in detail 10
 (b) Design CMOS logic gates for the following functions; 10
 (i) $Z = \overline{A.B.C.D}$
 (ii) $Z = \overline{A.(B+D) + C}$
7. Write notes on any two :- 20
 (a) IC resistors
 (b) IC capacitors
 (c) The twin tub process.