P4/RT-Ex-06-142

T.E. ETRX Sem VI

E. O.

22/05/06.

Con. 2844-06. **(REVISED COURSE)** **TV-8469**

(3 Hours) **[Total Marks : 100**

N.B. (1) Question No. **1** is **compulsory**.
(2) Solve any **four** from remaining **six**.

1. (a) Explain different addressing modes of pentium processor. Give suitable examples. **10**
   (b) Explain restoring division algorithm. Draw its flow chart. **5**
   (c) If a hard disk has 5 platters, 1024 tracks and 40 sectors, find its capacity. (Assume sector size 512 bytes). **5**

2. (a) What is Virtual Memory ? Explain how paging is useful in implementing Virtual Memory. **10**
   (b) With proper diagrams, explain various DMA transfer modes. **10**

3. (a) Explain concept of Cache memory with reference to principle of locality of reference, hit ratio and different Cache architectures. **12**
   (b) Show two way set associative mapping for following memory structure. **8**
   Cache size = 32 K Bytes
   Main memory size = 2 M Bytes
   Show the directory structure with no. of tag bits.

4. (a) Explain use of data structures like arrays, stack, queue and linked list. Compare with suitable example. **10**
   (b) Explain various methods of accessing the I/O devices. Also discuss the advantages and disadvantages of each method. **10**

5. (a) What is bus contention ? How is it resolved by using bus arbitration ? Explain in brief various bus arbitration schemes. **10**
   (b) Draw basic diagram for DRAM cell and for SRAM cell. Explain the same **10**

6. (a) Explain the concept of pipelined architecture. Show with suitable example that 5 stage pipelined architecture has 5 times speed up. **10**
   (b) State various formates of floating point numbers under IEEE 754 and convert $(27{\cdot}375)_{10}$ to long real format. **10**

7. Write short notes on (any **two**) :- **20**
   (a) Booth's Multiplication
   (b) Various methods of microprogram sequencing
   (c) Hazards in pipelined architecture.
