

(Library)

Logic Design

Con. 2734-07.

[REVISED COURSE]

ND-437

(3 Hours)

[Total Marks : 100]

N.B. : (1) Question 1 is compulsory.

(2) Attempt any four out of remaining six.

(3) Figures to the right indicate full marks.

(4) Assume suitable data if required.

1. (a) Compare PAL and PLA. 5
- (b) Draw Fax-OR gate using only all NAND gates and all NOR gates. 5
- (c) Draw a 3 bit Twisted Ring counter with neat waveforms. 5
- (d) (i) Convert $(0.61)_{10}$ to binary 1
- (ii) Convert $(0.111\ 01)_2$ to decimal 1
- (iii) Subtract $(0101)_2$ from $(0110)_2$. 1
- (iv) Perform $(1111)_2 \div (10)_2$. 1
- (v) Add $(4CE)_{16}$ and $(832)_{16}$. 1

2. (a) State and prove Demorgan's Law. 4
- (b) Simplify using boolean algebra – 9
 - (i) $y = \frac{(A + BC)(B + \bar{C}A)}{AD + \bar{C}\bar{D} \cdot \overline{BD + CD}}$
 - (ii) $y = AD + \bar{C}\bar{D} \cdot \overline{BD + CD}$
 - (iii) $y = ABC\bar{D} + AB\bar{C}D + ABCD + A\bar{B}CD$.
- (c) Convert $f(a, b, c) = \sum m(0, 1, 4, 7)$ into SOP form. 7

3. (a) Explain universal Shift Register. 5
- (b) Convert SR FF into JK flip-flop. 4
- (c) Convert T FF into JK flip-flop. 4
- (d) Explain Master-slave JK FF. 4
- (e) Explain Excitation Table of FF. 3

4. (a) Design mod-9 counter using JK flip-flop. 6
- (b) Differentiate between synchronous and Asynchronous counter. 6
- (c) Explain sequence generator using suitable example. 8

5. (a) Compare :- 8
 - (i) Encoder and decoder
 - (ii) Multiplex and demultiplexer.
- (b) Draw 2 line to 4 line decoder using NAND gates. 6
- (c) Realize following equation using mux $f(A, B, C) = \sum m(0, 3, 5, 7)$. 6

6. (a) Reduce $f(A, B, C, D) = \sum m(1, 3, 5, 9, 11, 13)$ by using k-map and realize using gates. 8
- (b) Explain QM method using suitable example. 6
- (c) Simplify using k-map. $f(A, B, C) = \sum m(0, 2, 4, 6)$. 6

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| 7. | (a) | Compare TTL, CMOS, ECL. logic families. | 6 |
| | (b) | Compare combinational and sequential circuits. | 6 |
| | (c) | Design full Adder and full subtractor. | 8 |
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