S.E. (Electronics) (Sem IV) (Rev) 22/5/07

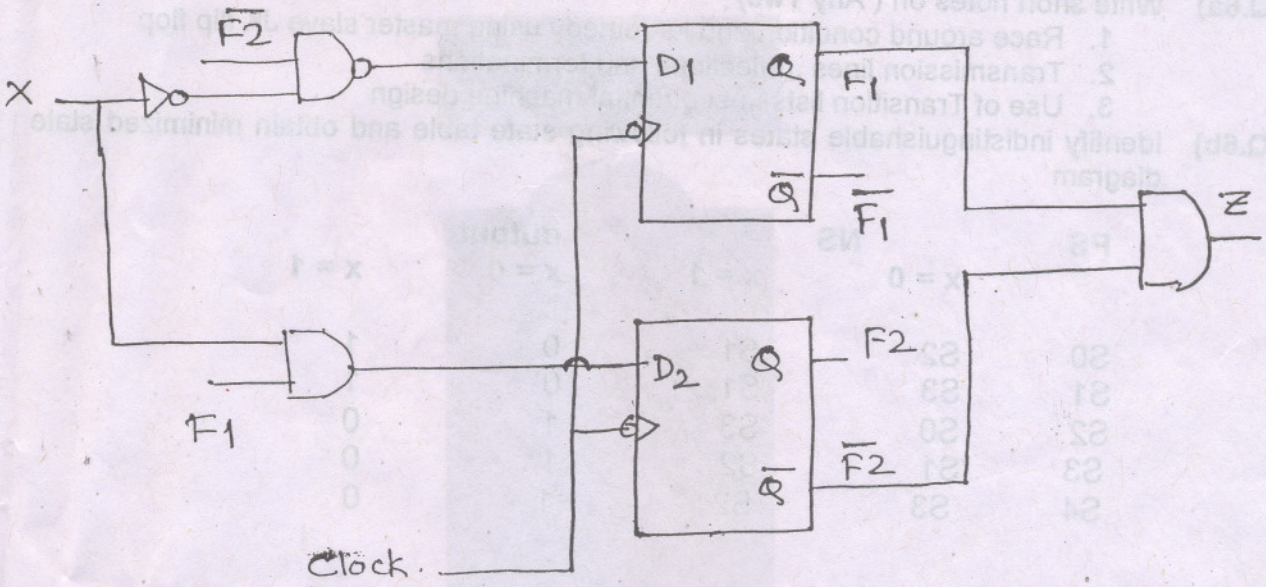
Digital Design II

Con/2652–07. (REVISED COURSE) ND–8159

(3 Hours) [Total Marks : 100

N.B. : (1) Question No. **1** is **compulsory**.
(2) Attempt any **four** questions from remaining **six** questions.

Q.1a) Analyze the sequential machine shown and obtain the state diagram for the same **10**



Q.1b) Write a VHDL code for a 8 bit left to right shift register with an enable input. **10**

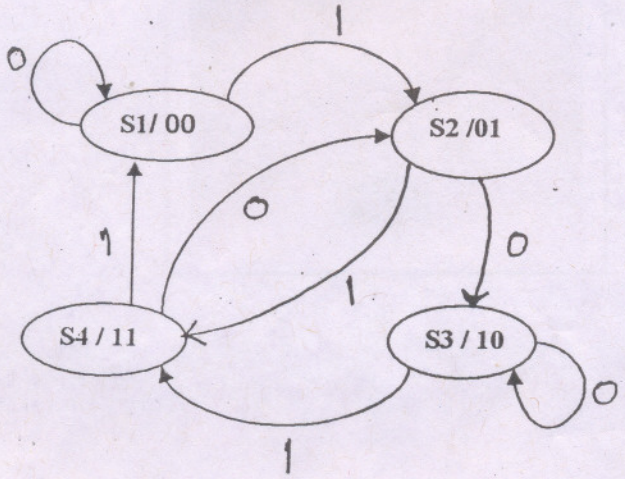
Q.2a) Design a finite state machine that acts as a 3 bit parity generator. For every three bits that are observed on the input W during three consecutive clock cycles , the FSM generates the parity bit P =1 if and only if the number of the ones in the three bit sequence is odd. Design machine as mealy machine. Use JK Flip flops and multiplexers for designing **12**

Q.2b) Explain what metastability is. State the circumstances under which a flip flop goes in a metastable state. What are the methods to overcome metastability problem? **08**

Q.3a) Using IC 74169 up /down counter and a few SSI / MSI devices design a counter which counts **10**

0 – 1 – 2 – 3 – 4 – 5 – 6 – 7 – 15 – 14 – 13 – 12 – 11 – 10 – 9 – 8 – 0

Q.3b) Write a VHDL code for following sequential machine whose state diagram is as shown **10**



Q.4a) What are different types of shift registers? Design a 4 bit Johnson counter using 74194 universal shift register **12**

Q.4b) Design a serial binary adder using flip flops Clearly show the steps for designing of sequential machine **08**

[TURN OVER

Q.5a) Draw and explain logic diagram of 64 X 1 diode ROM Use two dimensional decoding. **10**

Q.5b) Design a Mod 12 synchronous counter using T flip flop and logic gates. **10**

Q.6a) Write short notes on (Any Two) : **12**

1. Race around condition and its remedy using master slave JK flip flop
2. Transmission lines ,reflections and terminations
3. Use of Transition lists in sequential machine design

Q.6b) Identify indistinguishable states in following state table and obtain minimized state diagram **08**

PS	NS		output	
	x = 0	x = 1	x = 0	x = 1
S0	S2	S1	0	1
S1	S3	S1	0	1
S2	S0	S3	1	0
S3	S1	S2	1	0
S4	S3	S2	1	0

Q.7a) With reference to XC 9500 CPLD family answer the following questions : **12**

1. explain architecture of functional block
2. which are the analog controls available in I/O block of XC9500
3. What is the need of having variable no of pins, functional blocks and different types of packages in the family of devices.

Q.7b) Explain working of storage cell for one bit in a DRAM. Explain read, write and refresh operations. **08**