(3 Hours) [Total Marks : 100

N.B. : (1) Question No. **1** is **compulsory**.
(2) Attempt any **four** questions from remaining **six** questions.

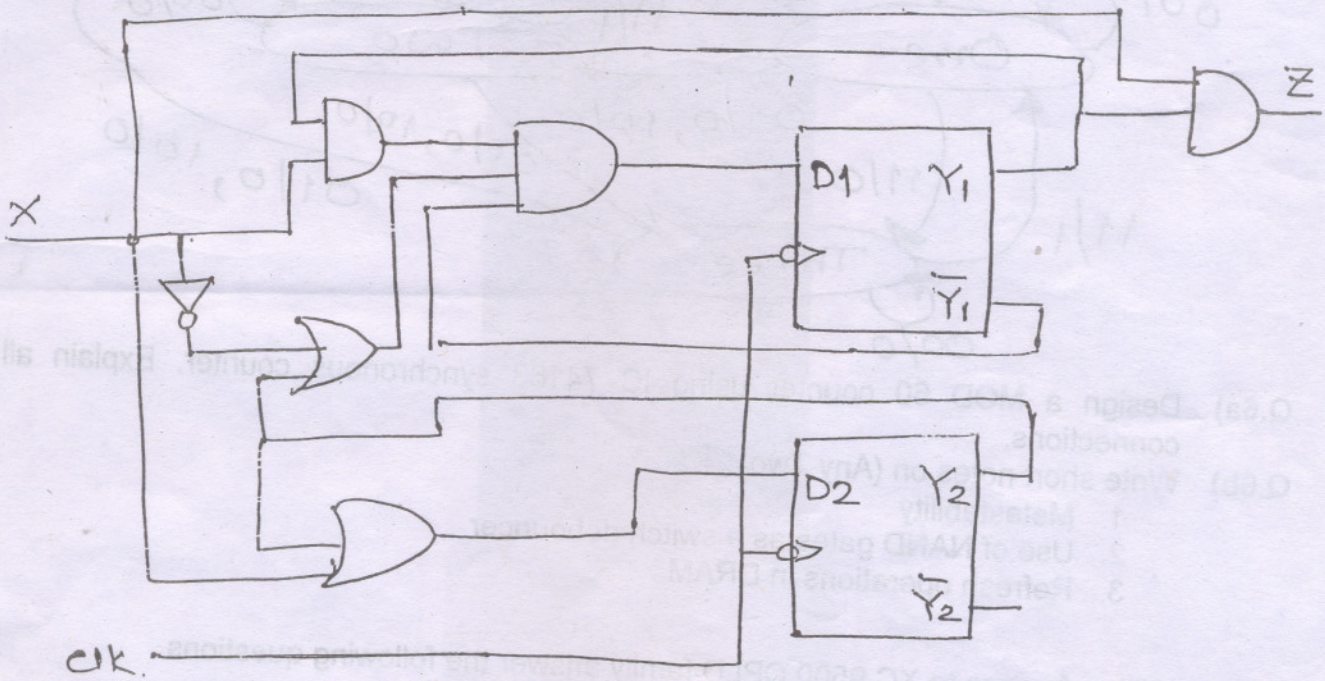
Q.1a) Design a clocked synchronous state machine with state output table given below. Use JK flip flops for synthesis **06**

Present State	Next State		O/P Z
	X = 0	X = 1	
A	B	D	0
B	C	B	0
C	B	A	1
D	B	C	0

Q.1b) What are asynchronous inputs? Explain preset and clear inputs in a flip-flop and their use. **06**

Q.1c) Write a VHDL code for 4-bit shift register (left to right shift) with external serial input. Write a behavioral architecture. **08**

Q.2a) Analyze the following clocked synchronous state machine. **10**



Q.2b) Write a VHDL code for serial binary adder. Using D F/F and Full adder as component. Write a structural architecture. **10**

Q.3a) What are ring counters and twisted ring counters? Design Johnson counter using IC 74194 universal shift register. **08**

Q.3b) Design a synchronous state machine for a candy dispenser mentioned below **12**

- Coin Inputs to dispenser are 50 p and 25 p
- Cost of candy is 1.25 Rs when this amount is deposited candy is given.
- The machine accumulates any extra money deposited and uses in the next transaction

Design a Mealy machine using D flip flops and NAND gates

Q.4a) Show how to use IC 7490 in different modes of operation Implement MOD 648 using IC 7490. **10**

Q.4b) Explain SRAM architecture block diagram with timing diagram for read and write operations. **10**

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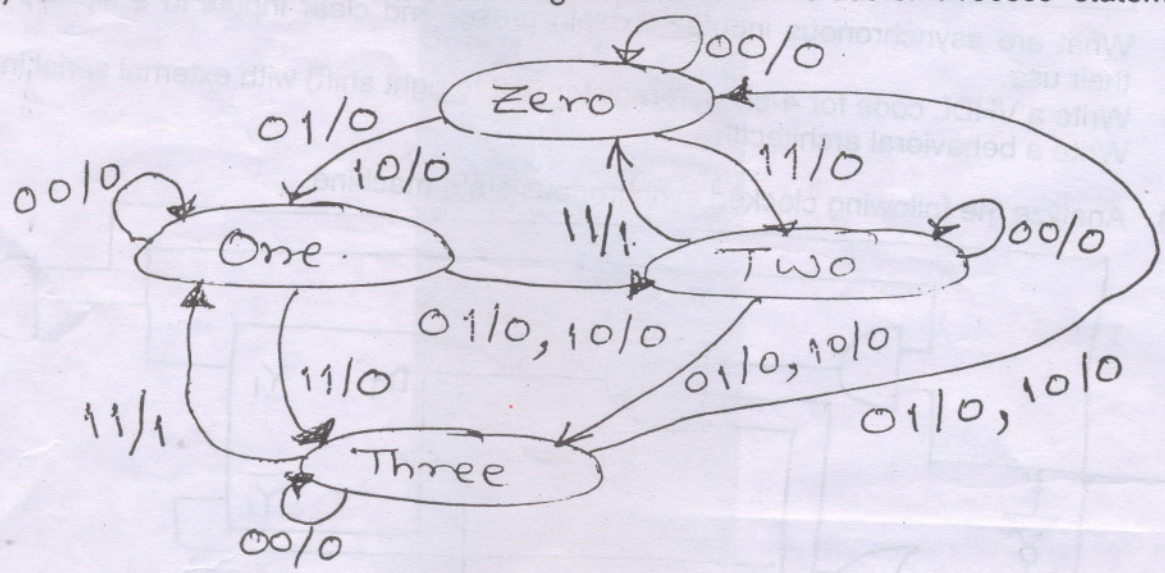
Q.5a) Reduce the following state table using Implication chart method and redraw the state diagram. **10**

Present State	Next State X = 0	Next State X = 1	Output X = 0	Output X = 1
S0	S3	S1	0	0
S1	S4	S0	0	1
S2	S6	S5	0	1
S3	S0	S3	1	0
S4	S0	S3	1	0
S5	S2	S1	0	0
S6	S0	S4	1	0

Q.5b) Write a VHDL code for the state Diagram shown. Make use of "Process" statement. **10**



Q.6a) Design a MOD 60 counter using IC 74163 synchronous counter. Explain all connections. **10**

Q.6b) Write short notes on (Any Two) **10**

1. Metastability
2. Use of NAND gates as a switch debouncer
3. Refresh operations in DRAM

Q.7a) With reference to XC 9500 CPLD family answer the following questions **10**

1. Explain architecture of functional block
2. Which are the analog controls available in I/O block of XC9500

Q.7b) Design a Moore Sequential machine that detects serial input sequence of X = "010110". Output Z goes high when such a sequence is detected. Use JK flip-flops and logic gates for the design. **10**